AM/CS/CYS/DS 124 (R-22)

Total No. of Questions : 10] [Total No.of Pages : 02

I/IV B. Tech. DEGREE EXAMINATIONS, AUGUST - 2024

Second Semester

AM / CS / CYS / DS

DIGITAL ELECTRONICS

Time : **Three Hours** Maximum : **70** Marks

Answer ONE Question from each Unit.

All Questions carry equal marks. 5x14=70 M

UNIT - I

1. a) Convert the following numbers to Octal :
   (i) $(1011.1010)_2$ (ii) $(BABA)_{16}$
   b) Perform the binary subtraction using 1's and 2's complement methods.
   $(110011)_2 - (1110011)_2$.

(OR)

2. a) What are universal gates realize AND, OR, NOT, EX-OR using NAND.
   b) Explain the theorems and properties of Boolean algebra.

UNIT - II

3. a) Minimize the following function using K-map and also verify through tabulation method.
   F (A, B, C, D) = Σm (1, 4, 5, 7, 8, 9, 12, 14) + d (0, 3, 6, 10).
   b) Convert the given expression in standard SOP form
   f (A,B,C) = AC + BA + BC.

(OR)

4. a) Simplify using k-map
   (i) (ABC)' + B'CD' + A'BD + ABCD + AC'D + A'BC'D'
   (ii) (AB)' + A'C + BC + AB + AC' + (ABC)' + ABC.
   b) Reduce using mapping the following expression and implement the real minimal expression in Universal logic. F = Σm (0, 2, 4, 6, 7, 8, 10, 12, 13, 15).

UNIT - III

5. a) Implement the Boolean function given below using 8X1 multiplexer
   f (A,B,C,D) = Σm (0, 2, 3, 5, 8, 11, 12, 14, 15).
   b) Design a 4-bit carry look ahead adder circuit.

P.T.O.

(OR)

6. a) Design a combinational circuit for a 2-bit magnitude comparator.

   b) Design a full subtractor circuit with basic gates.

UNIT - IV

7. a) Draw the logic diagram of a JK flip-flop and using truth table explain its operation.

   b) Reduce the number of states in the following state table and tabulate the reduced state table.

PS	NS, O/P	
	X=0	X=1
a	f, 0	b, 0
b	d, 0	c, 0
c	f, 0	e, 0
d	g, 1	a, 0
e	d, 0	c, 0
f	f, 1	b, 1
g	g, 0	h, 1
h	g, 1	a, 0

(OR)

8. a) Distinguish between combinational logic and sequential logic.

   b) Explain about sequential circuits, state table and state diagram.

UNIT - V

9. a) Explain the operation of a 4-bit shift register using RS flip-flops.

   b) Draw the logic diagram to implement 16 x 8 ROM and explain its architecture ?

(OR)

10. a) Explain in detail about synchronous counters.

    b) Implement the following Boolean functions using PAL.

W (A, B, C, D) = Σm (0, 2, 6, 7, 8, 9, 12, 13)

X (A, B, C, D) = Σm (0, 2, 6, 7, 8, 9, 12, 13, 14)