PULSE CIRCUITS & ICs LAB/EC261R22

II/IVB.TECH–IISEM

LABORATORY MANUAL

Prepared By

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BAPATLA WOMEN'S ENGINEERING COLLEGE::BAPATLA

AN ISO 9001-2015 CERTIFIED INSTITUTION

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COLLEGE VISION & MISSION

COLLEGE VISION:

BWEC has been established with forethought to organize the growing needs of higher technical education for WOMEN, to provide them a competitive edge and a unique niche in the society. We at BWEC are determined to create a conducive environment with updated technological inputs and latest information to facilitate the students with a pleasant feel in acquiring knowledge and skills required to make them globally competitive technocrats.

COLLEGE MISSION:

Our mission is to impart the quality education on par with global standards to the students from all over India, and particularly those from local and rural areas. We continuously try to maintain high standards to make them technologically competent and ethically strong individuals who shall be able to improve the quality of life and economy of our country.

DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

VISION

To produce highly professional and socially responsible women engineers through world class quality technical education and research to meet industry and Society needs in the field of Electronics and Communication Engineering.

MISSION

M1- To inculcate quality education for women through innovative learningpractices with the use of modern tools.

M2- To impart professional ethics and moral values through co-curricular andExtra-curricular activities as individual and team member.

M3- Empowering graduates through industrial trainings/on-job training in collaboration with

Industries with-a-view to life-long learning.

Programme Educational Objectives (PEO's)

PEO1: To develop and implementation of Electronics and Communication systems by imparting technical knowledge, professional leadership and communication skills as an individual and team in a multi-disciplinary stream.

PEO2: To train Graduates in solving complex problems, analyzing, designing and imparting research-based knowledge by using modern scientific tools to develop least cost-effective and innovative products.

PEO3: To produce women graduates through life-long learning, who ensure ethical and moral behavior.

Programme Specific Outcomes (PSO's)

PSO1: To understand and analyze basic concepts of electronics and communication in various areas like signal processing, VLSI, embedded systems, communications, digital and analog devices.

PSO2: Ability to design and develop computing systems using concepts of mathematics, electronics engineering and other related inter disciplines to asses and resolve societal, environmental, health safety and cultural issues with professional ethics.

Programme Outcomes (POs)

- **PO1: Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
- **PO2: Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- **PO3: Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

- **PO4: Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- **PO5: Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools prediction and modeling to complex engineering activities with an understanding of the limitations.
- **PO6: The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice
- **PO7: Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and the need for sustainable development.
- **PO8: Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- **PO9: Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- **PO10: Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and receive clear instructions.
- **PO11: Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in team, to manage projects and in multidisciplinary environments.
- **PO12: Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

EC261R22–Pulse Circuits & IC'sLaboratory 2023-2024(EVEN)

SYLLABUS

EC 261 (R22) PULSE CIRCUITS AND ICs LAB L T P M C
0 0 3 100 1.5

1. Obtain the Response of Linear Wave-Shaping Circuits.

2. Design of Astable multivibrator

3. Design of Positive and Negative clippers

4. Design of Positive and Negative clampers

5. Design and Verification of Schmitt Trigger (usingIC741).

6. Measurement of Op-amp Parameters.

7. Applications of Op-amp (Adder, Subtractor, Integrator, Differentiator).

8. Instrumentation Amplifier using Op-Amp.

9. Waveform Generation using Op-amp (Square, Triangular).

10. Design of Active Filters (LPF&HPF-First Order).

11. Application of 555 Timer (Astable, Monostable, Schmitt Trigger).

12. PLL using 565.

13. Design of IC Regulator using 723.

14. Design of VCO using 566.

15. D-A Converter (R-2R Ladder).

NOTE: A minimum of 10(Ten) experiments have to be performed and recorded by the candidate to attain eligibility for University Practical Examination

EC261R22–Pulse Circuits & IC'sLaboratory 2023-2024(EVEN)

LIST OF EXPERIMENTS

1. Obtain the Response of Linear Wave-Shaping Circuits.
2. Design of Astable multivibrator
3. Design of Positive and Negative clippers
4. Design of Positive and Negative clampers
5. Design and Verification of Schmitt Trigger (usingIC741).
6. Applications of Op-amp (Adder, Subtractor, Integrator, Differentiator).
7. Waveform Generation using Op-amp (Square, Triangular).
8. Design of Active Filters (LPF&HPF-First Order).
9. Application of 555 Timer (Astable, Monostable, Schmitt Trigger)
10. Instrumentation Amplifier using Op-Amp.

EXPERIMENT(S) BEYOND THE SYLLABUS

1. Sampling Gates

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COURSEOBJECTIVES:

The course should enable the students

1. To understand the response of Linear & Non-Linear Wave shaping circuits to different inputs.
2. To analyze the design and Operation of Multivibrator Circuits using transistor's and IC's.
3. To obtain knowledge on various types of Linear and Non-Linear Applications of Op-Amps
4. To understand the Design and Analyze the Active Filters and Applications of special ICS

COURSEOUTCOMES:

On successful completion of the course, students will be able to

CO.No	Course Outcome Statement	Bloom's Taxonomy Level
C261.1	**Understand** the response of Linear & Non-Linear Wave shaping circuits to different inputs.	**Understand**
C261.2	**Analyze** the design and Operation of Multivibrator Circuits using transistor's and IC's	**Analyze**
C261.3	**Obtain** knowledge on various types of Linear and Non-Linear Applications of Op-Amps, measurement of OP-AMP parameters and wave form generators using op amp IC -741	**Evaluate**
C261.4	**Analyze** the Active Filters and Applications of special ICS, IC-555 timer, IC 565-PLL and 566-VCO.	**Analyze**
C261.5	**Analyze** general purpose voltage regulator using IC -723 and D-A converter(R-2R Ladder)	**Analyze**

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Mapping of Course Outcomes with Program Outcomes and PSO's:

Cos	PO1	PO2	PO 3	PO 4	PO5	PO 6	PO 7	PO8	PO9	PO10	PO 11	PO12	PS01	PSO2
C261.1	3	2	1	2	-	-	-	-	1	1	-	1	3	2
C262. 2	3	2	1	1	-	-	-	-	2	2	-	2	2	2
C263.3	3	3	2	2	-	-	-	-	2	3	-	2	3	3
C264.4	3	3	2	1	-	-	-	-	3	2	-	2	3	3
C265.5	3	2	2	1	-	-	-	-	2	2	-	3	3	3
AVG	3	2.4	1.6	1.4	-	-	-	-	2	2	-	2	2.8	2.6

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : No Correlation

EC261R22–Pulse Circuits & IC's Laboratory

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Experiment(s) beyond syllabus:

1.	Sampling gates	89

1. Linear Wave Shaping

Aim:

i) To design a low pass RC circuit for the given cutoff frequency and obtain its frequency response.

ii) To observe the response of the designed lowpass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

iii) To design a high pass RC circuit for the given cutoff frequency and obtain its frequency response**.**

iv) To observe the response of the designed high pass RC circuit for the given square waveform for T<<RC, T=RC and T>>RC.

Apparatus Required:

Name of the Component/Equipment	Specifications/Rating	Quantity(No's)
Resistors	1KΩ 10KΩ,100KΩ	Each 1
Capacitors	0.1μF	1
CRO	(0-20MHz)	1
Functiongenerator	(1Hz-1MHz)	1
A/D Bread board Trainer	-	1
Connecting wires	-	-

Theory:

The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called "linear wave shaping". An ideal low pass circuit is one that allows all the input frequencies below a frequency called cutoff frequency $f_c$and attenuate allthoseabovethisfrequency.Forpracticallowpasscircuit(Fig.1)cutoffisset to occur at a frequency where the gain of the circuit falls by 3 dB from its maximum at very high frequencies the capacitive reactance is very small, so the output is almost equal to the input and hence the gain is equal to 1. Since circuit attenuates low frequency signals and allows high frequency signals with little or no attenuation, it is called a high pass circuit.

Circuit Diagrams:

Low Pass RC Circuit:

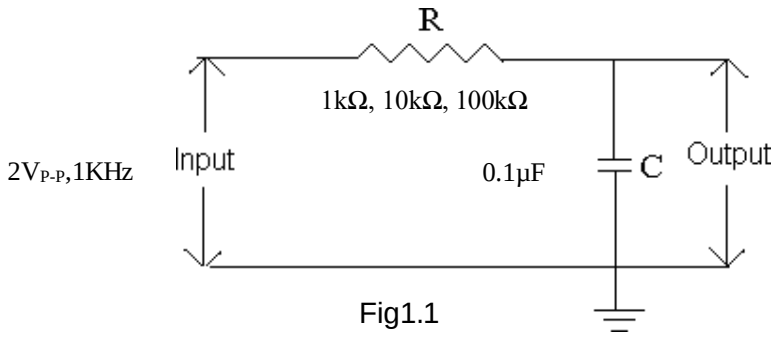


Fig1.1

High Pass RC Circuit:

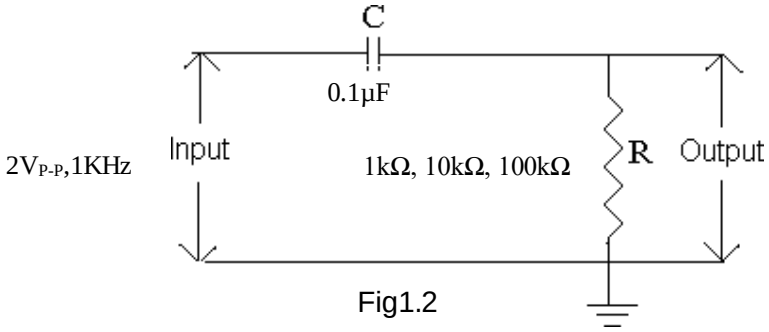


Fig1.2

Procedure:

A) Frequency response characteristics:

1.Connect the circuit as shown in Fig.1and apply as sinusoidal signal of amplitude Of 2V p-p as input.

2. Vary the frequency of input signal in suitable steps100Hz to1MHz and note down the p-p amplitude of output signal.

3. Obtain frequency response characteristics of the circuit by finding gain at each frequency and plotting gain in dB vs frequency.

4. Find the cutoff frequency $f_c$by noting the value of fat 3 dB down from the maximum gain

B) Response of the circuit for different time constants:

Time constant of the circuit RC=0.0198ms

1. Apply as square wave of 2vp-p amplitude as input.
2. Adjust the time period of the wave forms of that T>>RC,T=RC,T<<RC and observe the output in each case.
3. Draw the input and output waveforms for different cases.

Sample readings

Low Pass RC Circuit Input Voltage : $V_i=2V_{(p-p)}$

Observations:

Low Pass RC Circuit :

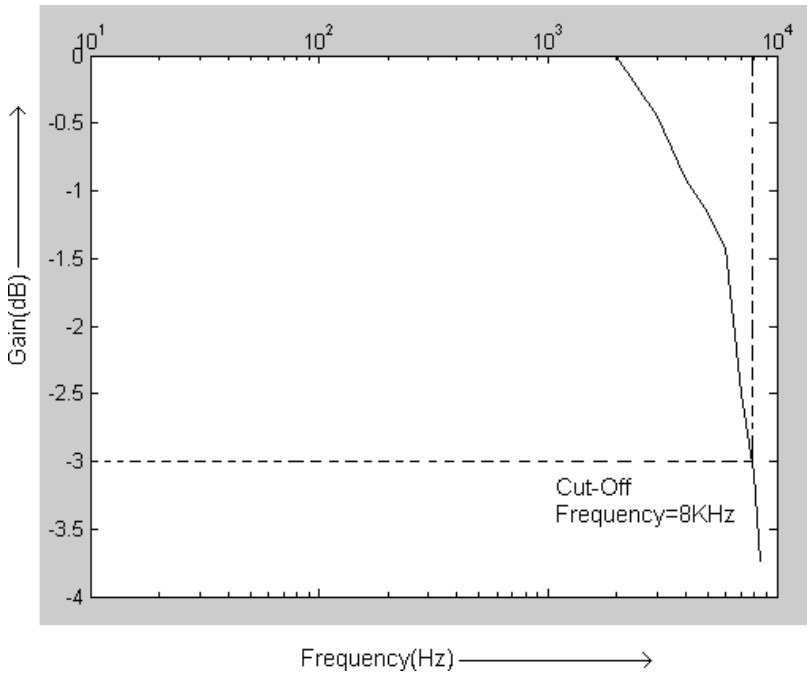
S.No	Frequency (Hz)	O/PVoltage,V_o (V)	Gain=20log(Vo/Vi) (dB)

High Pass RC Circuit:

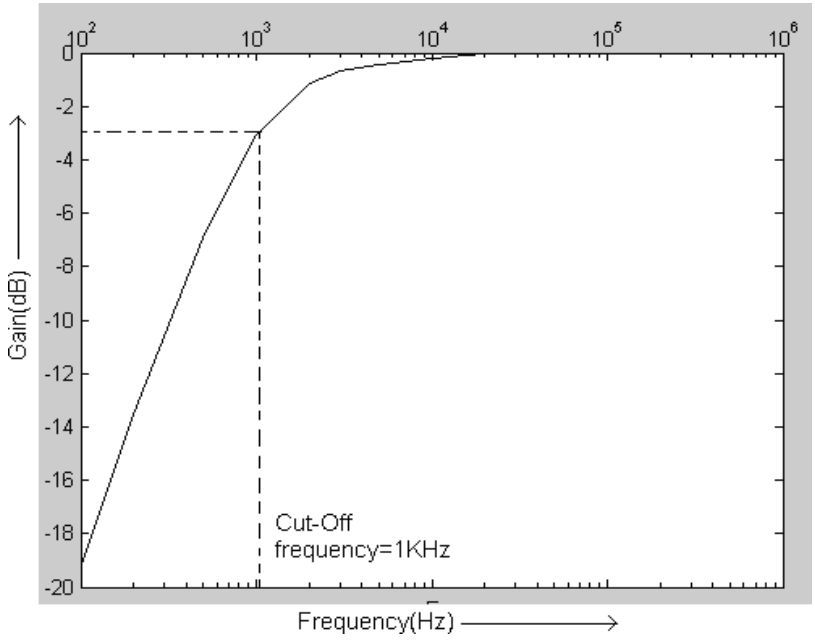
S.No	Frequency(Hz)	O/PVoltage,V_o(V)	Gain=20log(Vo/Vi)(dB)

Model Graphs and waveforms:

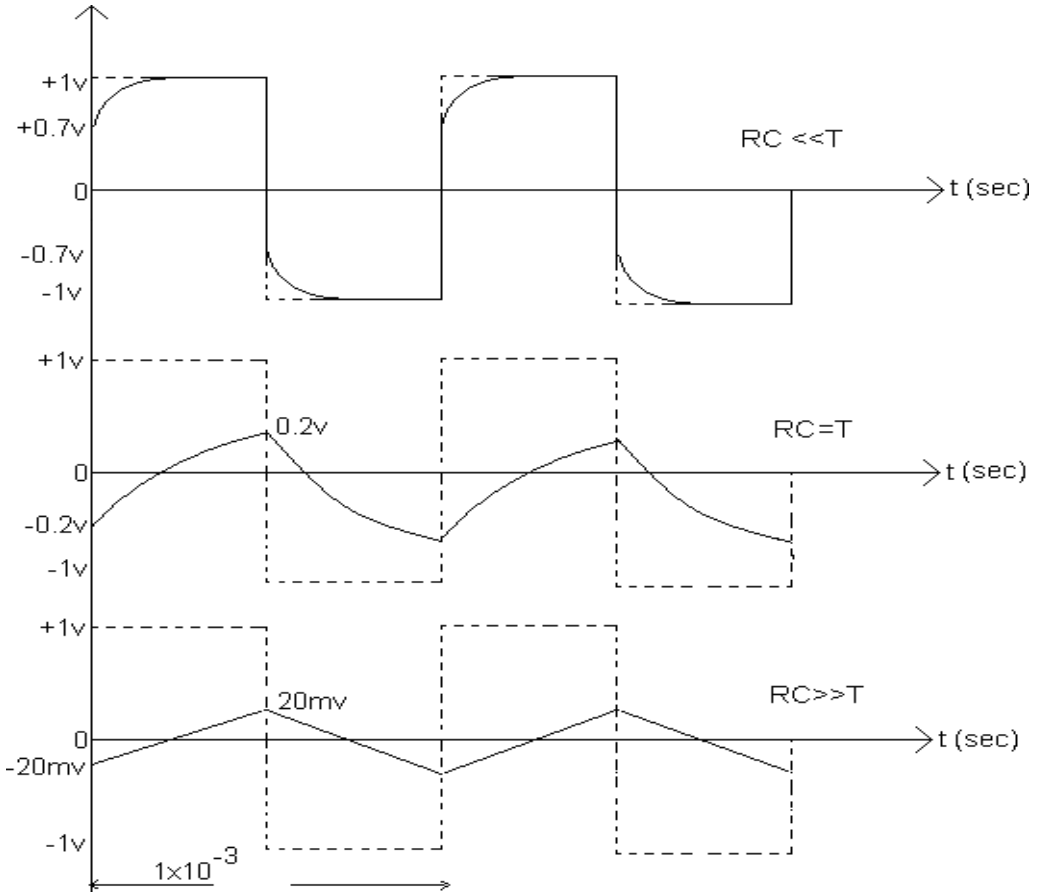
Low Pass RC circuit frequency response:



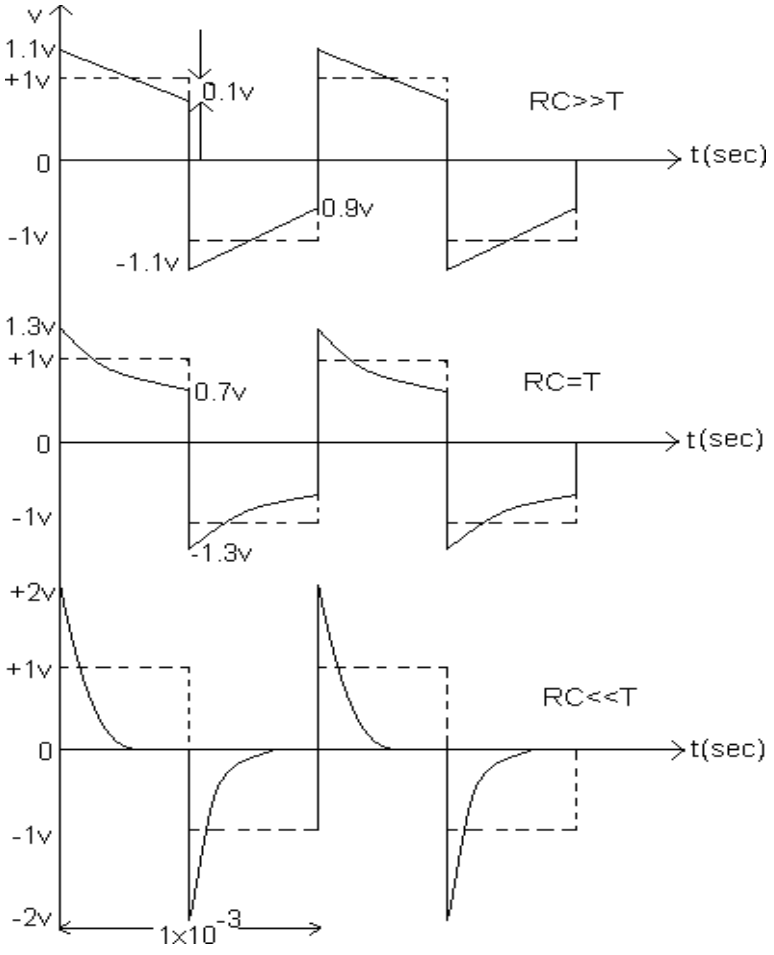
High Pass RC circuit frequency response:



HighPassRCcircuit:



Low Pass RC circuit:



Precautions:

1. Connections should be made carefully**.**
2. Verify the circuit connections before giving supply.
3. Take readings with out any parallax error.
4. Connections should be made carefully**.**
5. Verify the circuit connections before giving supply.
6. Take readings with out any parallax error.

Result: RC lowpass and high pass circuits are designed, frequency response and response at different time constants is observed.

Inference: At low frequencies the capacitor C behaves almost like an open circuit and output is equal to input voltage. As the frequency increases the reactance of the capacitor increases and C functions almost like a short circuit and output voltage is equal to zero. So the low pass RC allows low frequency signals and stops high frequency signals. When the time constant of the circuit is less than the time period of an input signal, the capacitor charges and discharges quickly. So the shape of the output is same as the input signal. But asthetimeconstantofcircuitisincreasesthecapacitorchargesanddischargesveryslowly so when the time constant of the low pass RC circuit is very much greater than the time period of a input signal acts as an integrator.

Viva-Voce Questions:

1. What is linear wave shaping?
2. How low pass RC circuit works as an integrator?
3. How low pass RC circuit works as differentiator?
4. Define time constant.
5. Define tilt.
6. Explain the output wave forms of high pass and low pass circuit for different conditions.

2. Astable Multivibrator usingTransistors

Aim: To Observe the ON& OFF states of transistor in an Astable Multivibrator.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Transistor(BC107)	BC107	2
Resistors	1KΩ,100KΩ	2
Capacitor	0.01μF	2
Regulated Power Supply	(0-30)V, 1A	1
Cathode Ray Oscilloscope	(0-20MHz)	1
Function generator	(1Hz-1MHz)	1

Theory:

Astable multivibrator: An Astable Multivibrator has two quasi stable states and it keeps on switching between the set wo states by itself. No external triggering signal is needed. The astable multivibrator cannot remain in definitely in anyone of the two states. The two amplifier stages of an astable multivibrator are regenerative across coupled by capacitors. The astable multivibrator may be to generate a square wave of period, 1.38RC.

Circuit Diagram:

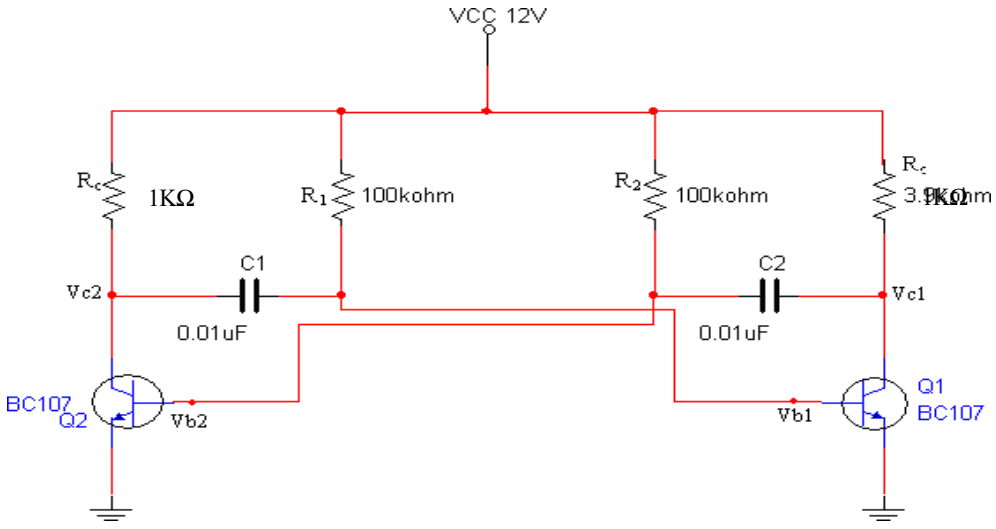


Fig 2.1:AstableMultivibrator

Procedure:

1. Calculate the theoretical frequency of oscillations of the circuit.
2. Connect the circuit as per the circuit diagram shown in Fig1.
3. Observe the voltage waveforms at both collectors of two transistors simultaneously.
4. Observe the voltage waveforms at each base simultaneously
   with corresponding collector voltage as shown in Fig3.
5. Note down the values of waveforms carefully.
6. Compare the theoretical and practical values.

Calculations:

Theoretical Values:

$RC=R_1C_1+R_2C_2$

Time Period,T=1.368RC

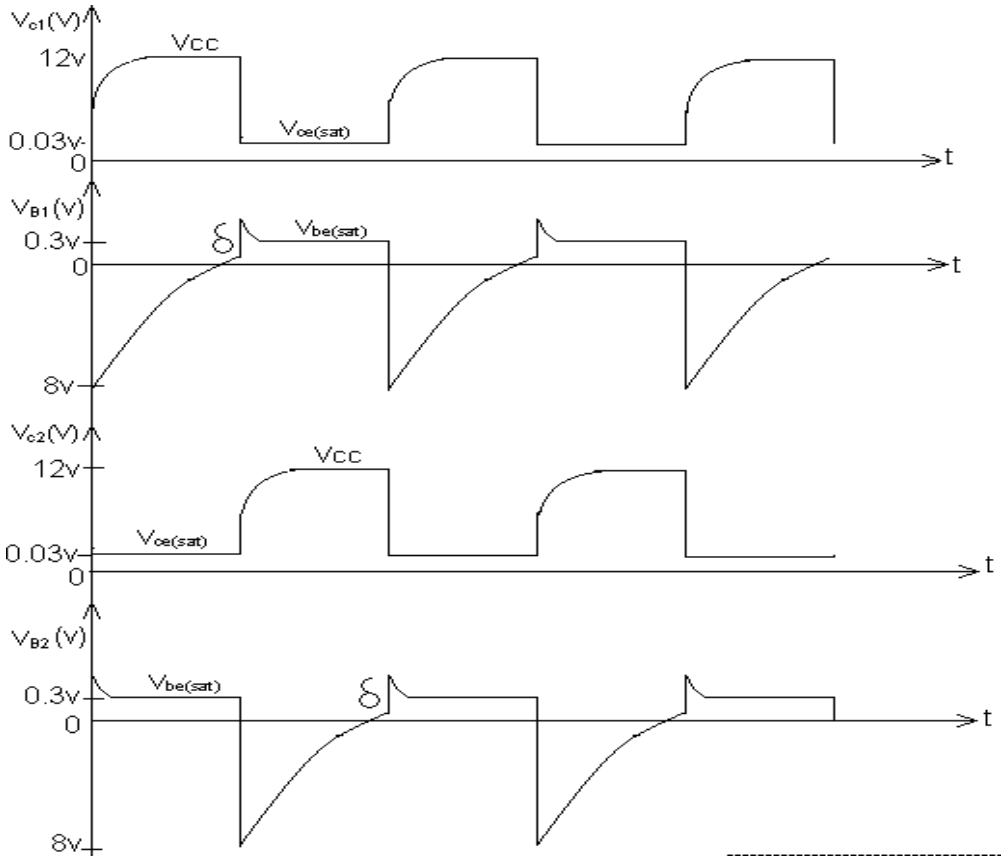
$=1.368x100x10^{3}x0.01x10^{-6}$

$=93\mu sec$

$= 0.093$ m sec

Frequency,f=1/T=10.75KHz

Model wave forms:



Precautions:

1. Connections should be made carefully.
2. Readings should be noted with out parallax error.

Result: The wave forms of astable multivibrator have been verified

Viva Questions:

1. What do mean by duty cycle?
2. What are the applications of astable multivibrator?
3. How many stable states we have in astable multivibrator?
4. What is quasi stable state?

3.Design of positive and negative Clippers

Aim: To obtain the output and transfer characteristics of various diode clipper circuits.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	10KΩ	1
Diode	1N4007	1
Cathode Ray Oscilloscope	20MHz	1
Function generator	(1Hz-1MHz)	1
Regulated power supply	(0-30)V,1A	1

Theory:

The basic action of a clipper circuit is to remove certain portions of the Waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

Circuit diagrams:

Positive peak clipper with reference voltage,V=2V:

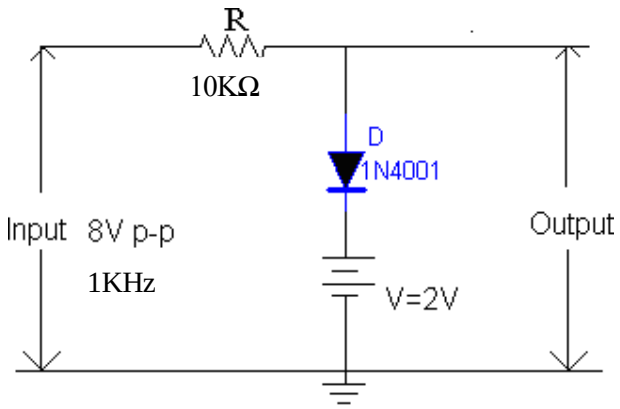


Fig 3.1

Positive Base Clipper with Reference Voltage,V=2V:

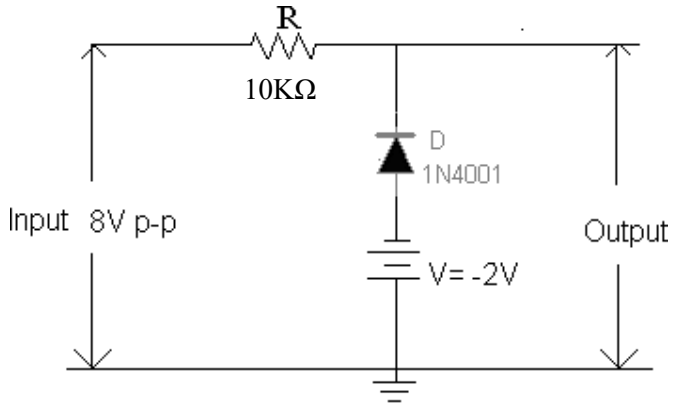


Fig 3.2

Negative Base Clipper with Reference Voltage,V=-2V:

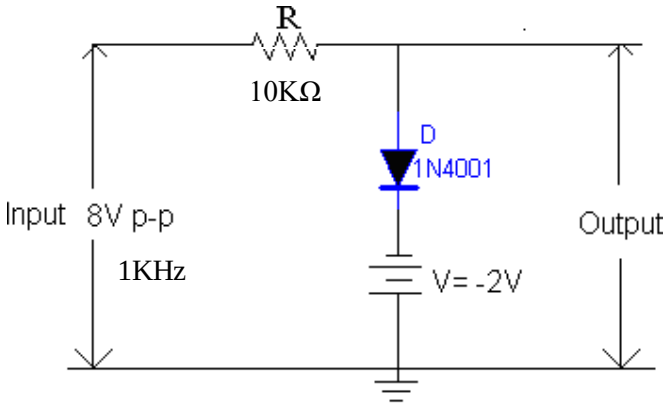


Fig 3.3

Negative peak clipper with reference voltage,V=-2v:

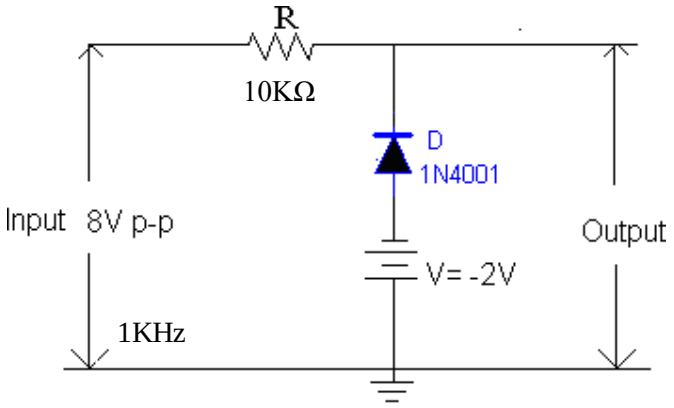


Fig 3.4

Slicer Circuit:

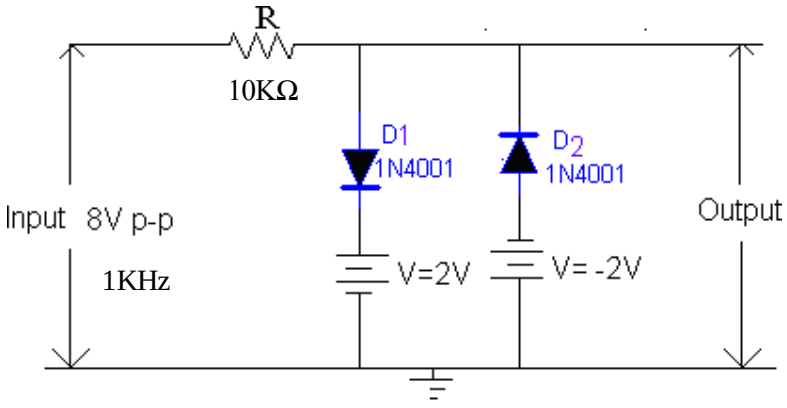


Fig 3.5

Procedure:

1. Connect the circuit as per circuit diagram shown in Fig.1
2. Obtain a sine wave of constant amplitude 8Vp-p from function generator and apply as input to the circuit.
3. Observe the output waveform and note down the amplitude at which clipping occurs.
4. Draw the observed output waveforms.
5. To obtain the transfer characteristics apply dc voltage at input terminals and vary the voltage insteps of 1V up to the voltage level more than the reference voltage and note down the corresponding voltages at the output.
6. Plot the transfer characteristics between output and input voltages.
7. Repeat the steps1 to 5 for all other circuits.

Sample Readings:

Positive peak clipper: Reference voltage,V=2V

S.No	I/p voltage (v)	O/p voltage (v)

Positive base clipper: Reference voltage V=2V

S.No	I/p voltage(v)	O/p voltage(v)

Negative base clipper: Reference voltage=2V

S.No	I/p voltage(v)	O/p voltage(v)

Negative peak clipper: Reference voltage=2V

S.No	I/p voltage(v)	O/p voltage(v)

Slicer Circuit:

S.No	I/p voltage(v)	O/p voltage(v)

Theoretical calculations:

Positive peak clipper:

V_r=2v,Vγ=0.6v

When the diode is forward biased $V_o=V_r+ V\gamma$

=2v+0.6v

=2.6v

When the diode is reverse biased the $V_o=V_i$

Positive base clipper:

V_r=2v,Vγ=0.6v

When the diode is forward biased Vo=Vr–Vγ

=2v-0.6v

=1.4v

When the diode is reverse biased $V_o=V_i$.

Negative base clipper:

V_r=2v,Vγ=0.6v

When the diode is forward biased V_o=-V_r+ Vγ

=-2v+0.6v

=-1.4v

When the diode is reverse biased V_o=V_i.

Negative peak clipper:

V_r=2v,Vγ=0.6v

When the diode is forward biased V_o=-(V_r+Vγ)

=-(2+0.6)v

=-2.6v

When the diode is reverse biased V_o=V_i.

Slicer:

When the diode D1 is forward biased and D2 is reverse biased V_o=V_r+ Vγ

=2.6v

When the diode D2 is forward biased and D2 is reverse biased V_o=-(V_r+ Vγ)

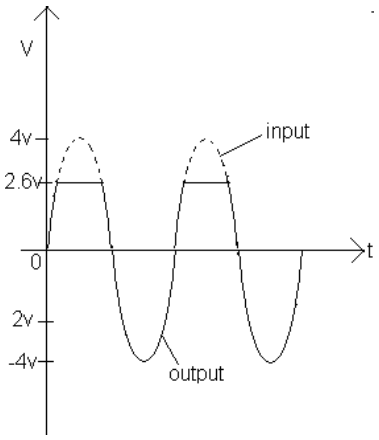
=-(2+0.6)v

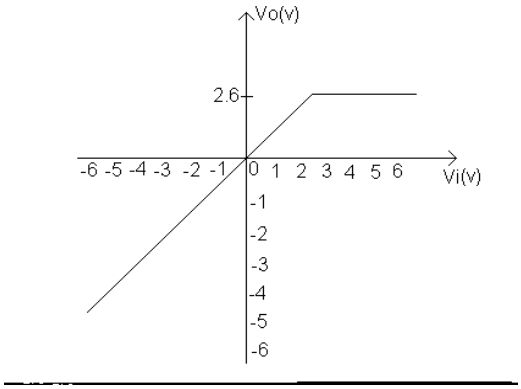
=-2.6v

When the diodes D1&D2 are reverse biased V_o=V_i.

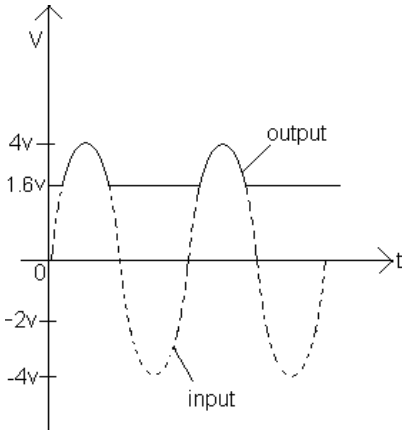
Model wave forms and Transfer characteristics:

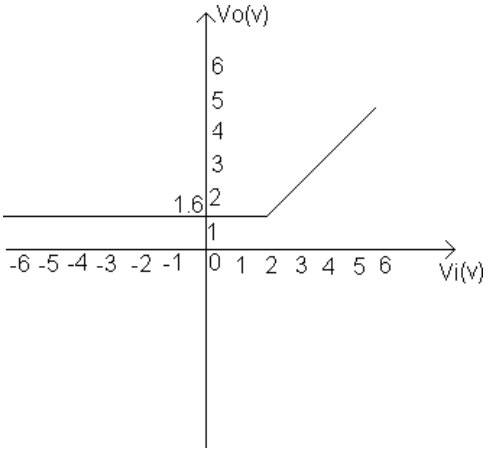
Positive peak clipper: Reference voltage=2V



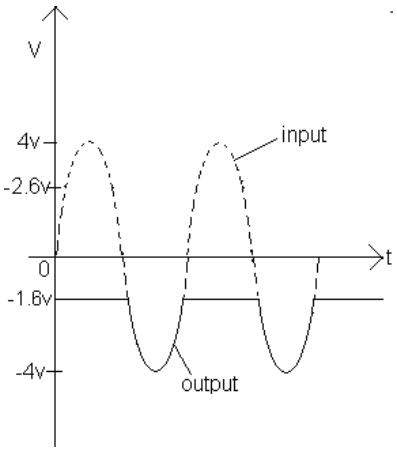


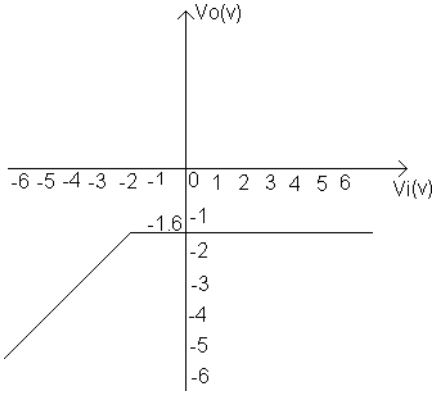
Positive base clipper: Reference voltage=2V



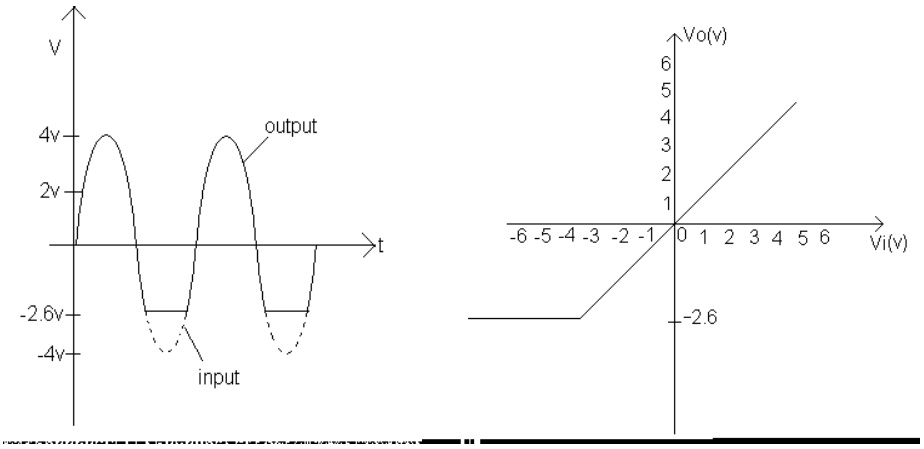


Negative base clipper: Reference voltage=2v

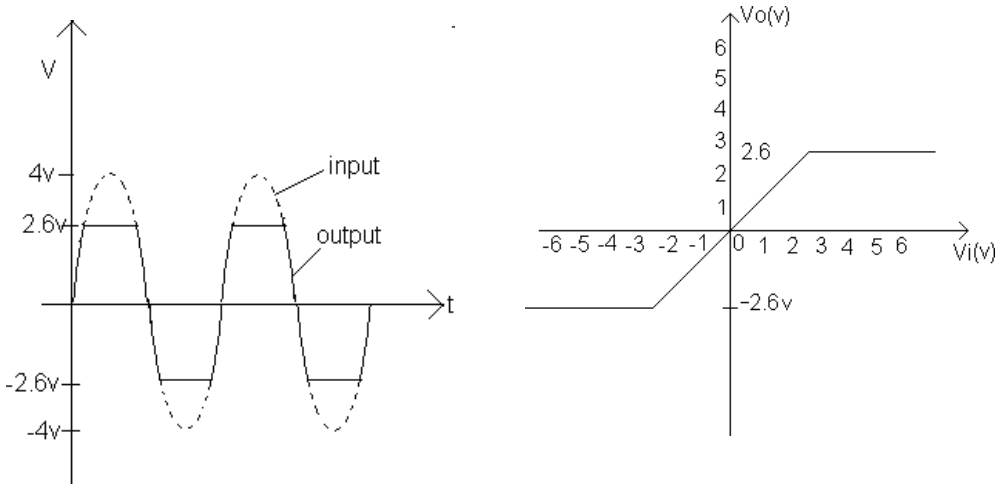




Negative peak clipper: Reference voltage=2V



Slicer Circuit:



Precautions:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

Result:

Performance of different clipping circuits is observed and their transfer characteristics are obtained.

Inference:

The clipper circuit's clips off the some part of the waveform depend on the applied reference voltage. Clipping circuits do not require energy storage elements these circuits can also use as sine to square wave converter at low amplitude signals.

.

Viva-Voce Questions:

1. What is clipper?
2. What are the different types of clippers?
3. What are the different applications of clipper?
4. What is two level clipper?
5. Explain the operation of positive and negative clipper?

4.Design of positive and negative Clampers

Aim: To verify the output of different diode clamping circuits.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	10KΩ	1
Capacitor	0.47uF	1
Diode	1N4007	1
Cathode Ray Oscilloscope	(0-20MHz)	1
Function generator	(1Hz-1MHz)	1
Regulated power supply	(0-30)V, 1A	1

Theory:

The circuits which are used to add a DC level as per the requirement to the AC signals are called clamper circuits. Capacitor, diode, resistor are the three basic elements of a clamper circuit. The clamper circuits are also called DC restorer or DC inserter circuits. The clampers are classified as

1. Negative clampers
2. Positive clampers

Circuit Diagrams

Positivepeakclampingto0V:

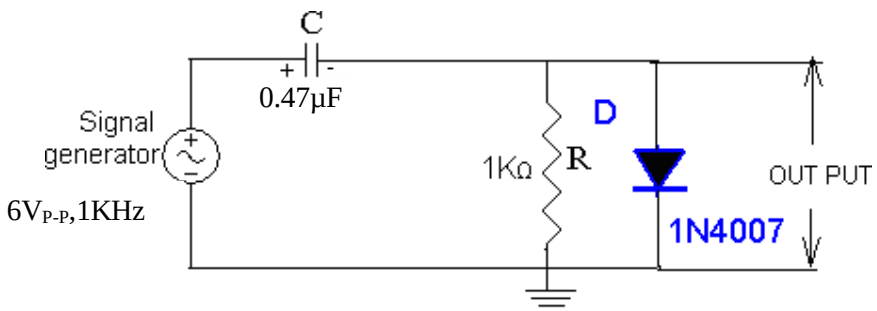


Fig 4.1

Positive peak clamping to V_r=2v

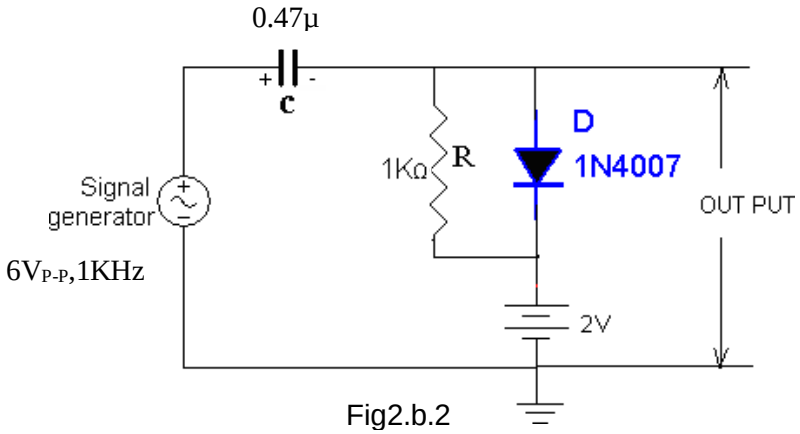


Fig2.b.2

Negative peak clamping toV_r=0v

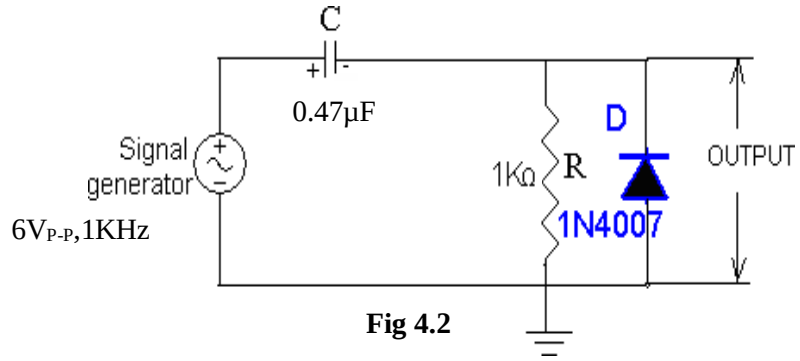


Fig 4.2

Negative peak clamping to V_r=-2v

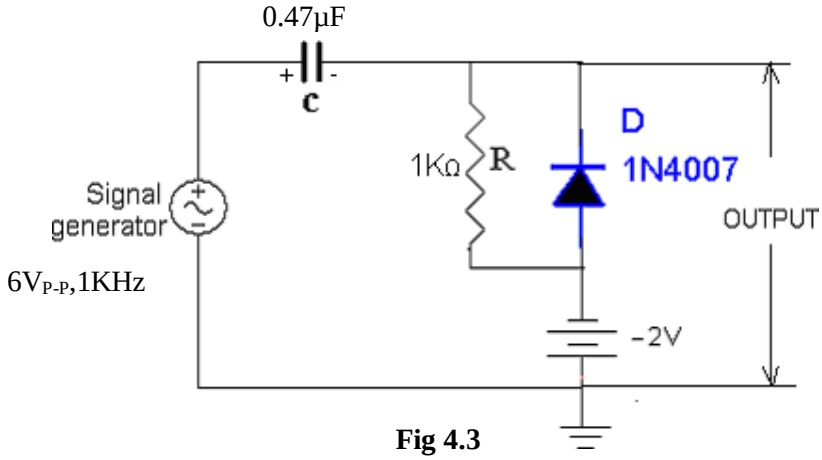


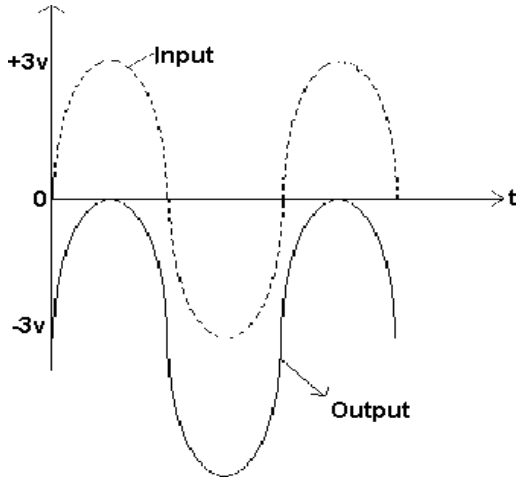
Fig 4.3

Procedure:

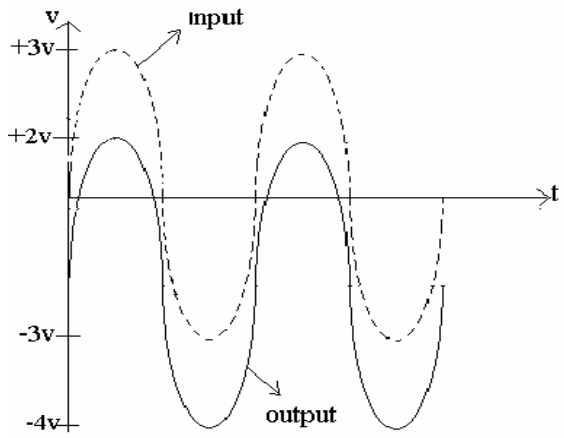
1. Connect the circuit as per circuit diagram.
2. Obtain a constant amplitude sine waveform function generator of 6Vp-p, frequency of 1KHz and give the signal as input to the circuit.
3. Observe and draw the output waveform and noted own the amplitude at which clamping occurs.
4. Repeat the steps 1 to 3 for all circuits.

Model wave forms:

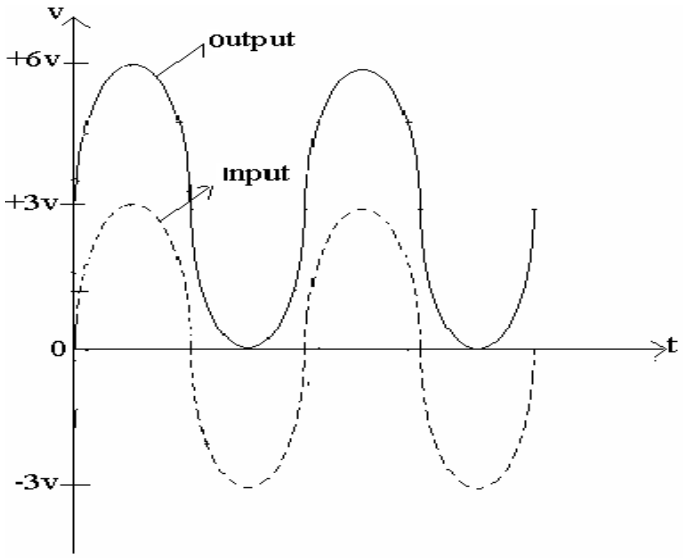
Positive peak clamping to 0V:



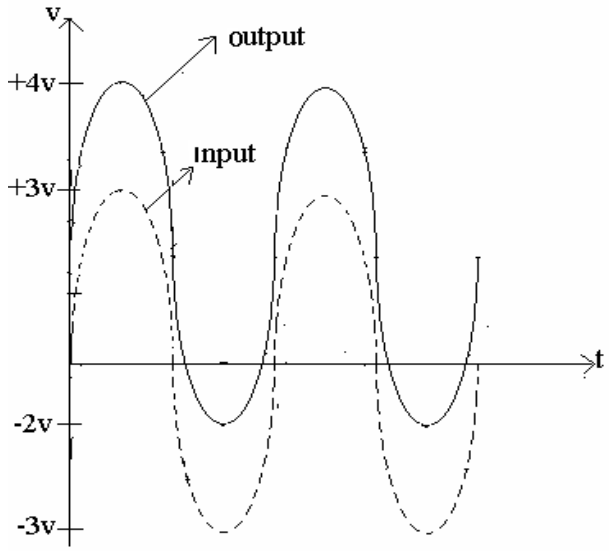
Positive peak clamping to V_r=2V



Negative peak clamping to 0V



Negative peak clamping to Vr =-2V



Precautions:

1. Connections should be made carefully.
2. Verify the circuit before giving supply.
3. Take readings without any parallax error.

Result:

Different clamping circuits are constructed and their performance is observed.

Inference:

In positive peak clamping, Positive peak of the sinusoidal wave form is clamped to 0v when reference voltage is 0v, and clamped to 2v when reference voltage is 2v. That is the waveform is shifted to negative side. So we called this clamper as negative clamper. In negative peak clamping, negative peak of the sinusoidal waveform is clamped to 0v when reference voltage is 0v, and clamped to -2v when reference voltage is -2v. That is the waveform is shifted to positive side. So we called this clamper as positive clamper.

Viva Questions:

1. What are the different types of clamping circuits?
2. What are the different applications of clampers?
3. Why clamper is called DC inserter?
4. Explain the operation of positive clamper and negative clamper?

5.Schmitt Trigger Circuits using IC741

Aim: To design the Schmitt trigger circuit using IC741.

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	IC741	Refer	1
2	Cathode Ray Oscilloscope	(1Hz-20MHz)	1
3	Resistors	100Ω 5.6KΩ	2 1
4	Regulated power supply	(0-30)V, 1A	1

Theory:

The circuit shows an inverting comparator with positive feedback. This circuit converts arbitrary wave forms to a square wave or pulse. The circuit is known as the Schmitt trigger (or) squaring circuit. The input voltage V_{in}changes the state of the output $V_o$every time it exceeds certain voltage levels called the upper threshold voltage $V_{ut}$and lower threshold voltage V_{lt}.

When V_o=-V_{sat},the voltage across $R_1$is referred to as lower threshold voltage, V_{lt}. When V_o=+V_{sat}, the voltage across R_1 is referred to as upper threshold voltage V_{ut}.

The comparator with positive feedback is said to exhibit hysteresis, a dead band condition.

Circuit Diagrams:

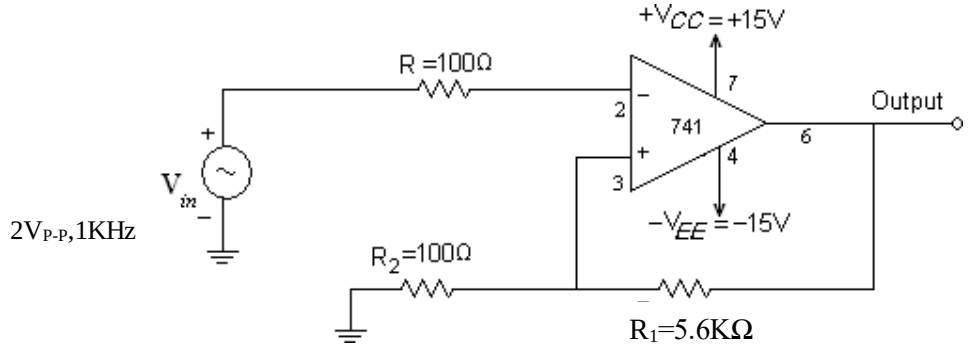


Fig5.1Schmitt trigger circuit using IC741

Design:

$V_{utp}=[R_1/(R_1+R_2)](+V_{sat})$

$V_{ltp}= [R_1/(R_1+R_2)](-V_{sat})$

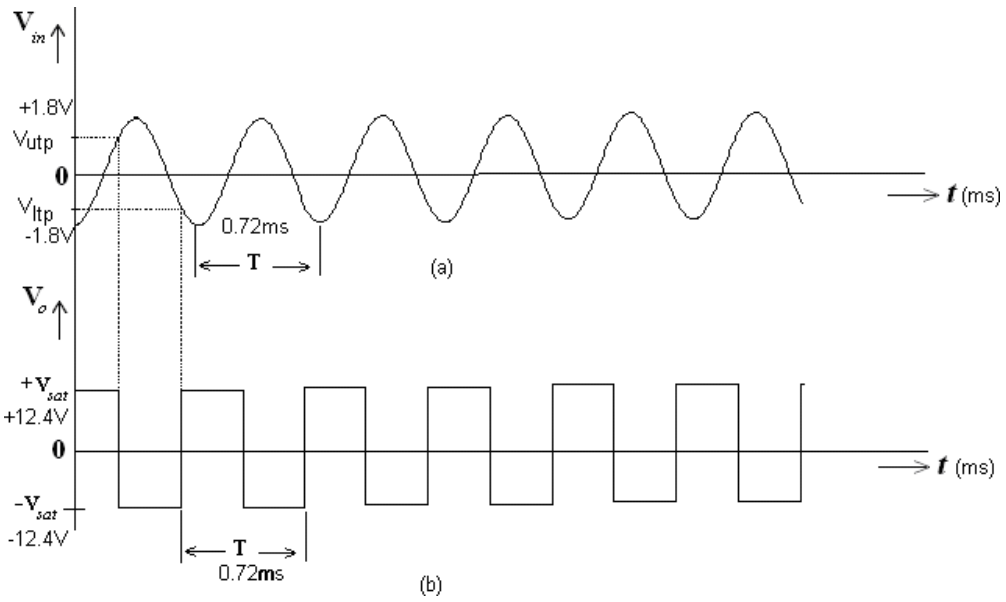
$V_{hy}=V_{utp}–V_{ltp}$

$=[R_1/(R_1+R_2)][+V_{sat}–(-V_{sat})]$

Procedure:

1. Connect the circuit as shown in fig.
2. Apply an arbitrary waveform(sine/triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.
3. Observe the output at pin6 of the IC741Schmitt trigger circuit by varying the input and note down the readings as shown in Table 1 and Table2
4. Find the upper and lower threshold voltages(V_{utp},V_{Ltp}) from the output waveform.

Waveforms:



Schmitt trigger input and output waveforms

Sample readings:

Table1:

Parameter	Input		Output	
	741		741	
Voltage(V_{p-p})				
Time period(ms)				

Table2:

Parameter	741
V_{utp}	
V_{ltp}	

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result:

UTP and LTP of the Schmitt trigger are obtained by using IC741 as shown in Table2.

Inferences: Schmitt trigger produces square waveform from a given signal.

Viva Questions:

1. What do mean by Schmitt trigger?
2. What are the different applications Schmitt triggers?
3. What is meant by Hysteresis voltage?
4. What is meant by threshold voltage?

6. Measurement of op-Amp parameters

Aim: To measure the op-Amp parameters such as

(a) Input Bias Current

(b) Input Offset current

(c) Input off set voltage of given op-Amp

(d) Slew Rate

Apparatus:

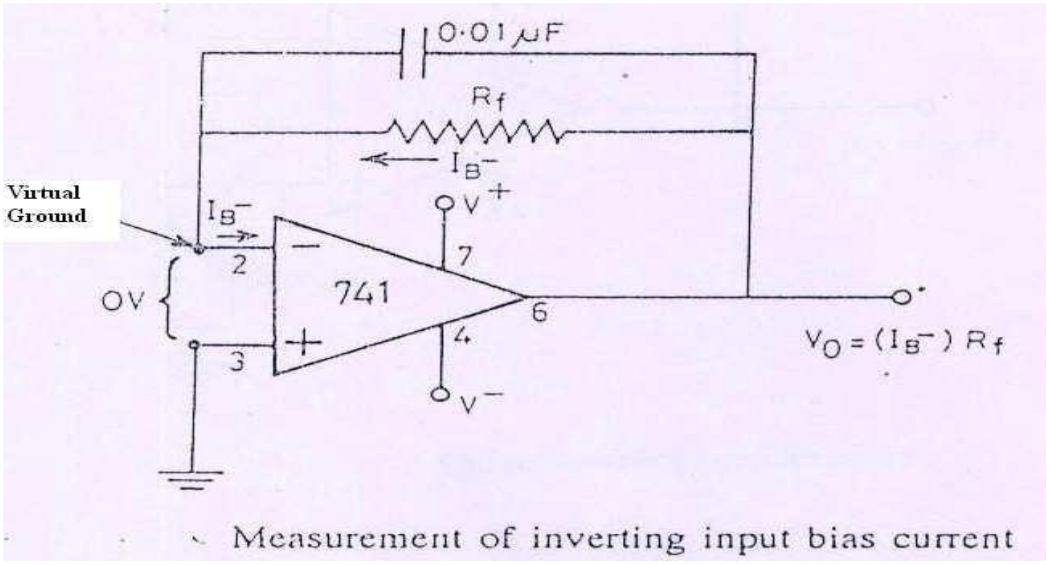
- 741 Op-Amps
- Sine wave Signal generator
- Resistors, capacitors
- 10KΩ,100Ω,1MΩ,0.01uF

Procedure:

1. Set up the circuit shown in fig 6.1 to measure I_B
2. Set up the circuit shown in fig 6.2 to measure I_B^+.
3. Select the large resistor (in MΩ) and measure the output voltage.
4. Calculate $I_b = \frac{V_0}{R_f}, I_b^+ = \frac{V_0}{R}$
5. Calculate $I_B=(I_B^+ + I_B^-)/2$
6. Set up the circuit shown in fig1.3 to measure offset current loss.I_{os}=Vo/Rf.
7. Set up the circuit shown in fig1.4 $V_0=(1+R_f/R_i)V_{OS}+I_{OS}R_f=(1+R_f/R_i)V_{os}$
8. Set up the circuit shown in fig1.5
9. Adjust the input sine-wave signal generator so that the output is 1Vpeak sine wave at IKHz.
10. Slowly increase the input signal frequency until the output gets just distorted.
11. Calculate slew rate, $SR=2\pi fV_m/10^6 V/\mu S$ where V_m=peak output amplitude in volts and f= frequency in Hz.
12. Now give a square-wave input and repeat step-9 increase the i/p frequency slowly until the output is just barely a triangular wave. The SR= AVo/At V/j is where $V_0$is the change in the output voltage amplitude in volts, At = time required for AVo inj.is.

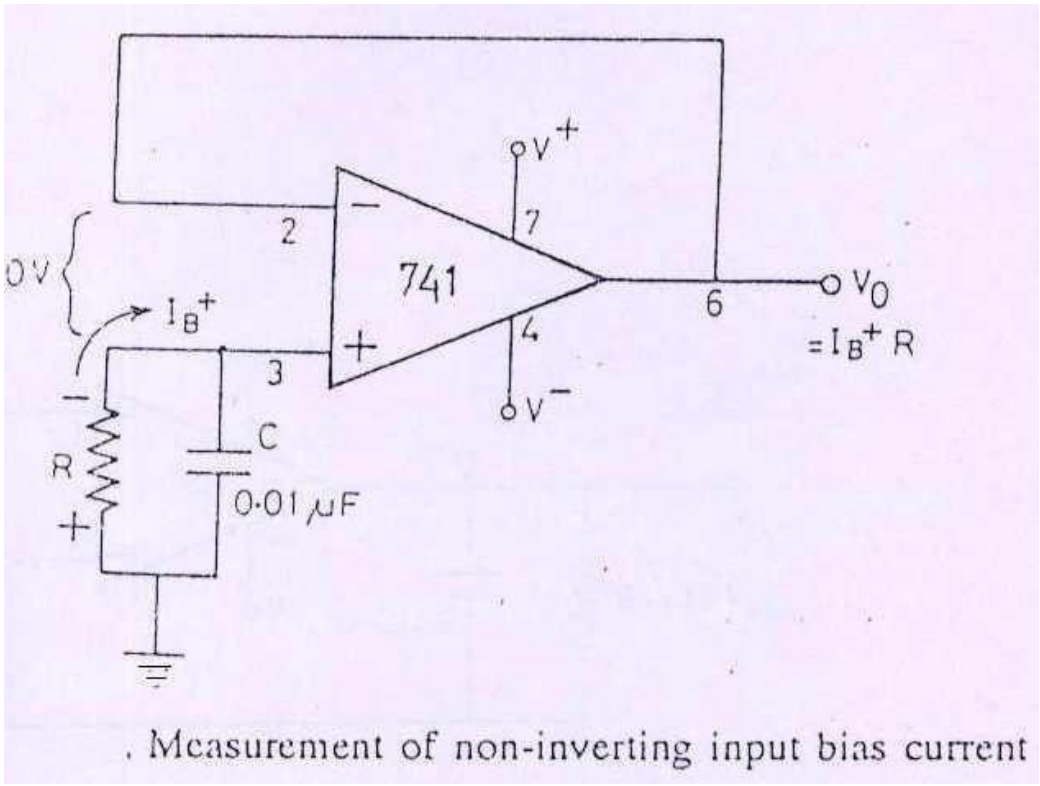
Precautions:

1. Don't disturb the setup while performing experiment.
2. Take the readings without parallax error



Measurement of inverting input bias current

Fig6.1



. Measurement of non-inverting input bias current

Fig6.2

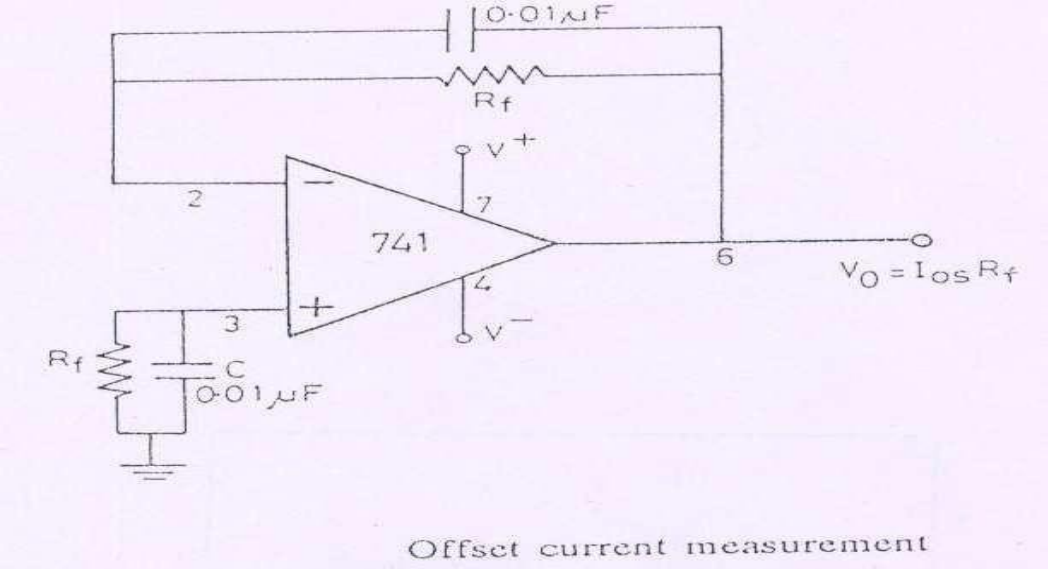


Fig6.3

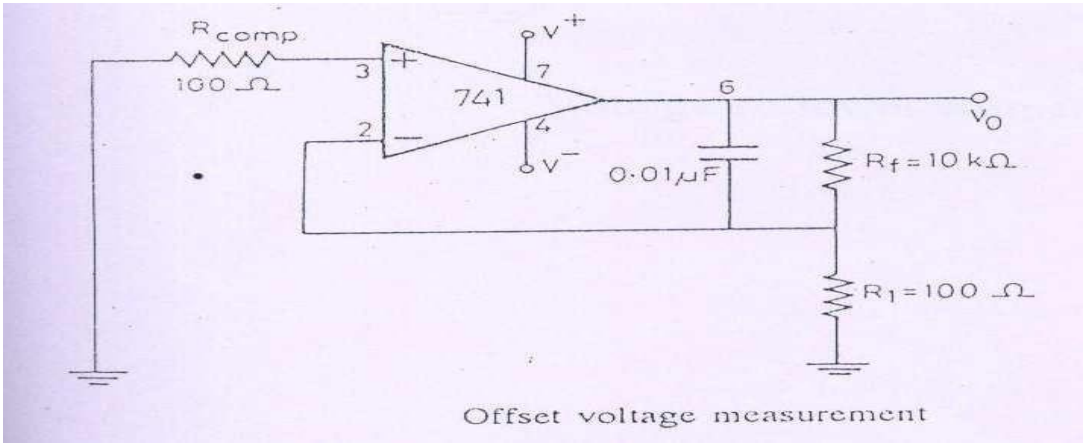
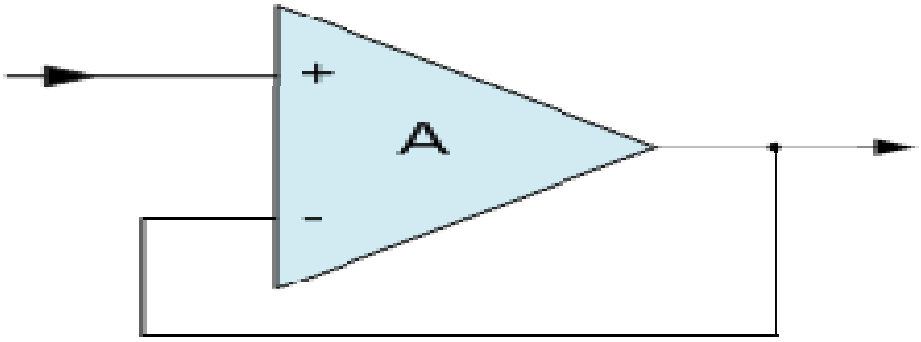


Fig:6.4

Vidt



Result:

Op Amp Parameters Are Measured Using 741 IC.

Viva Questions:

1. What are the ideal characteristics of an OP-AMP?
2. Define OP-AMP.
3. What do you mean by CMRR?
4. Define slew rate.

7.Applications of Op-Amp

Aim: To design adder for the given signals by using operational amplifier and to design integrator and differentiator for a given input (square/sine)

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC741	Refer AppendixA	1
2	Capacitors	0.01µf	2
3	Resistors	10kΩ 1kΩ 100kΩ	2 3 1
4	Regulated Power Supply	(0–30)V,1A	2
5	Function Generator	(1Hz-1MHz)	1
6	Cathode Ray Oscilloscope	(1Hz-20MHz)	1
7	Multimeters	$3^{½}$digitdisplay	2

Theory

Adder*:* A two input summing amplifier may be constructed using the inverting mode. The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called "virtual ground", i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

Integrator: In an integrator circuit, the output voltage is the integration of the input voltage.

The output voltage of an integrator is given by $V_o=-1/R_1C_f \int_o^t Vidt$

At low frequencies the gain becomes infinite ,so the capacitor is fully charged and 0behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor

Differentiator: In the differentiator circuit the output voltage is the differentiation of the Input voltage. The output voltage of a differentiator is given by V_o $=-RfC_1$ $\frac{dV_{in}}{df}$.The input Impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.

For pin configuration and specifications of op-amp(IC741),refer Appendix-B

Circuit Diagrams:

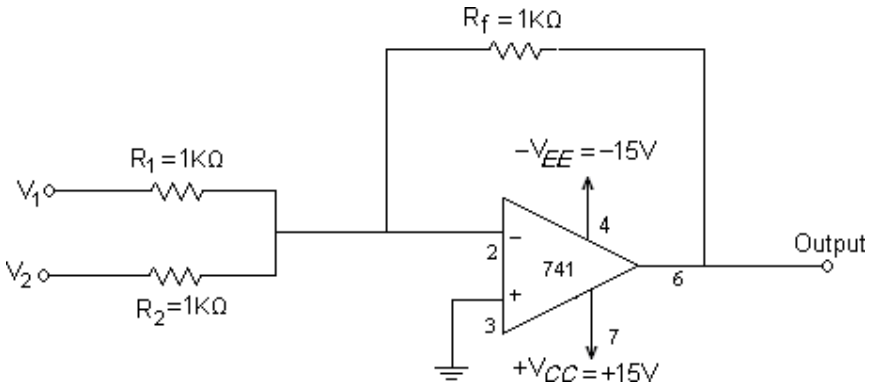


Fig7.1:Adder

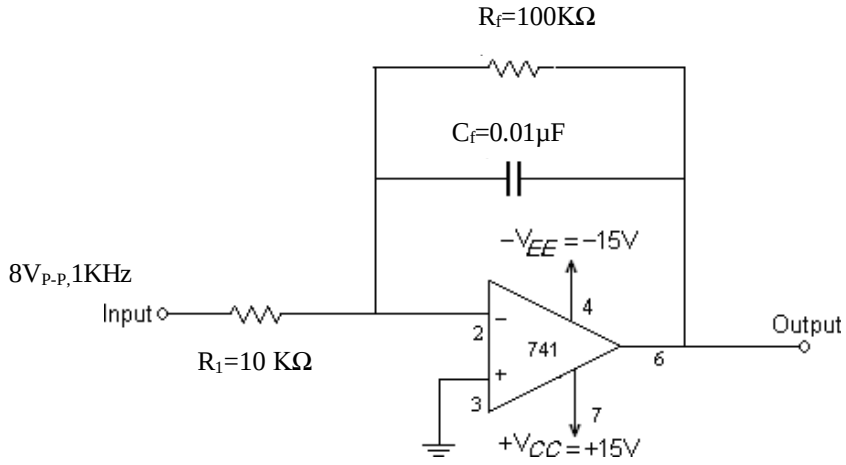


Fig7.2:Integrator

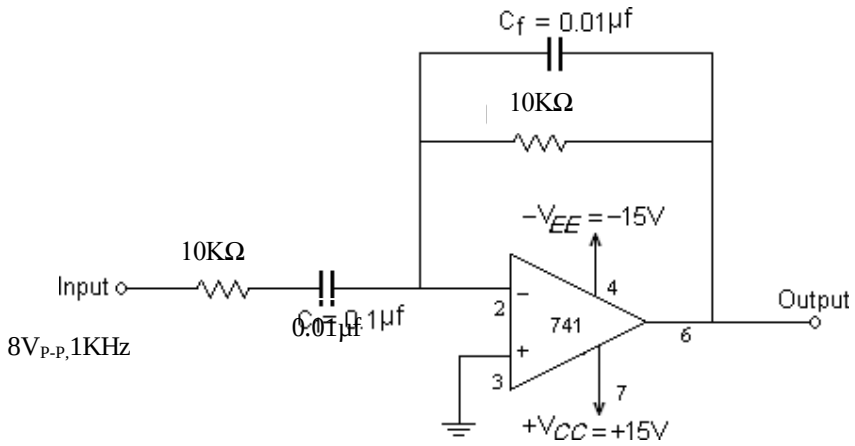


Fig7.3:Differentiator

Design equations:

Adder:

Output voltage, $V_o=-(V_1+V_2)$

Subtractor:

Output voltage vo=(v1-v2).

Integrator:

Choose $T=2\pi R_fC_f$

Where T= Time period of the input signal

Assume $C_f$and find R_f

Select $R_f=10R_1$

$$V_{o(p-p)}= \frac{-1}{R_1C_f}\int_o^{T/2} V_{i(p-p)}dt$$

Differentiator

Select given frequency $f_a= 1/(2\pi R_fC_1)$, Assume C_1 and find R_f

Select $f_b= 10\ f_a= 1/2\pi R_1C_1$ and find R_1

From $R_1C_1=R_fC_f$, find C_f

Procedure:

Adder:

1. Connect the circuit as per the diagram shown in fig7.1.
2. Apply the supply voltages of ±15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown in fig7.1.
4. Apply two different signals (DC/AC) to the inputs
5. Vary the input voltages and note down the corresponding output at pin6 of the IC 741 adder circuit.
6. Notice that the output is equal to the sum of the two inputs.

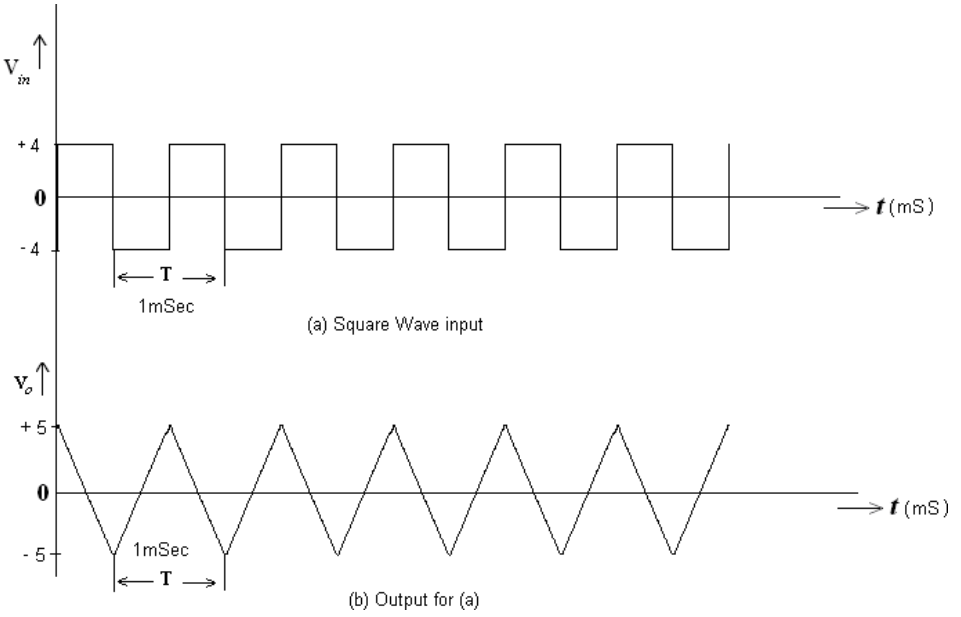
Integrato r

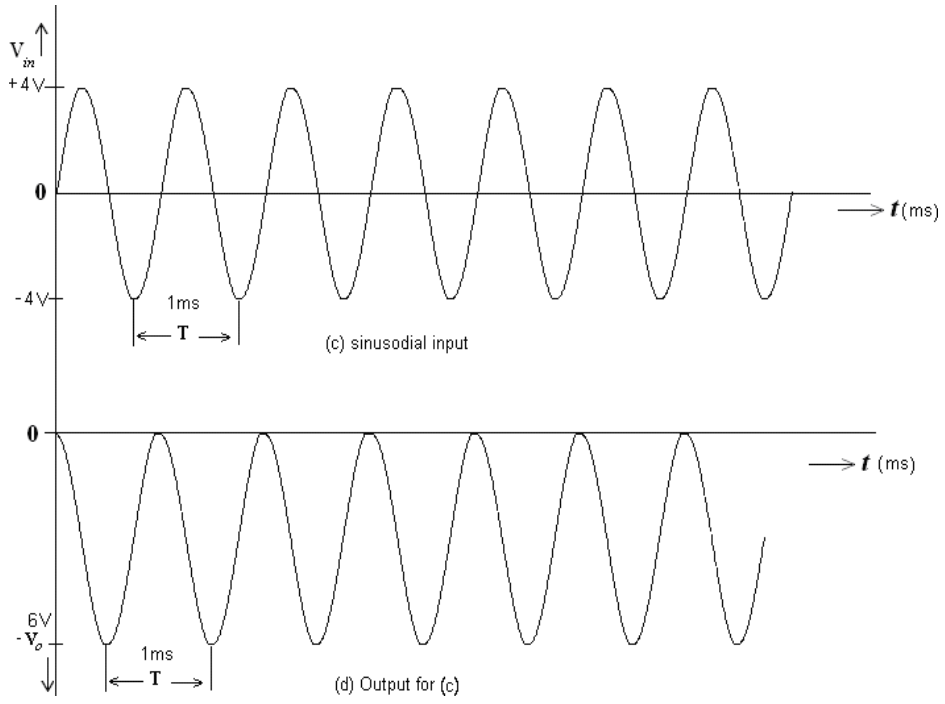
1 Connect the circuit as per the diagram shown in fig7.2
2 Apply a square wave/sine input of 4V(p-p) of 1KHz
3 Observe the o/p at pin6.
4 Draw input and output waveforms as shown in fig:7(a)

Differentiator

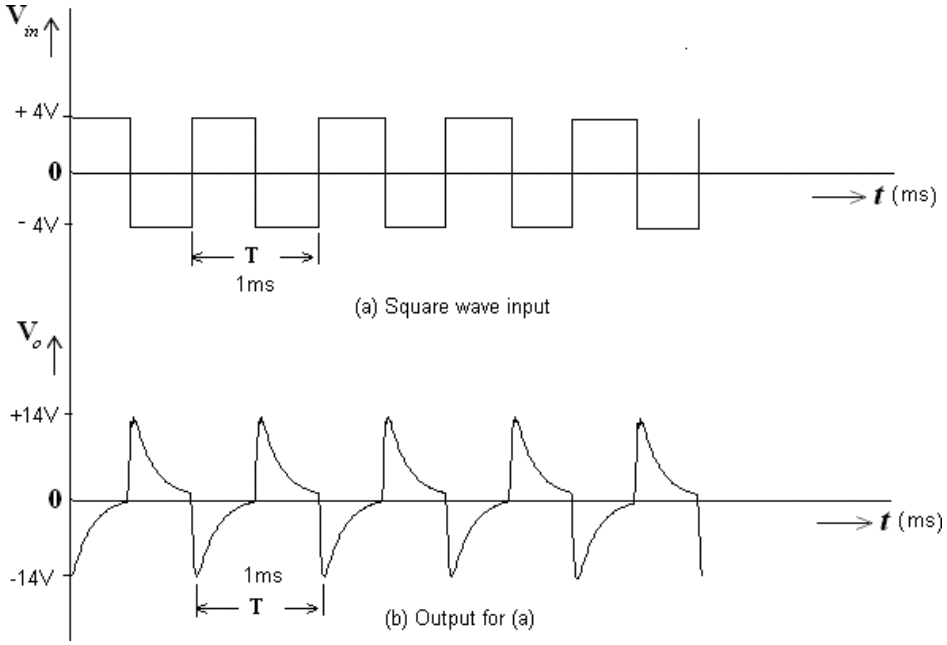
1. Connect the circuit as per the diagram shown in fig7.3
2. Apply a square wave/sine input of 4V(p-p)of 1KHz
3. Observe the output at pin6
4. Draw the input and output waveforms as shown in fig:7(b)

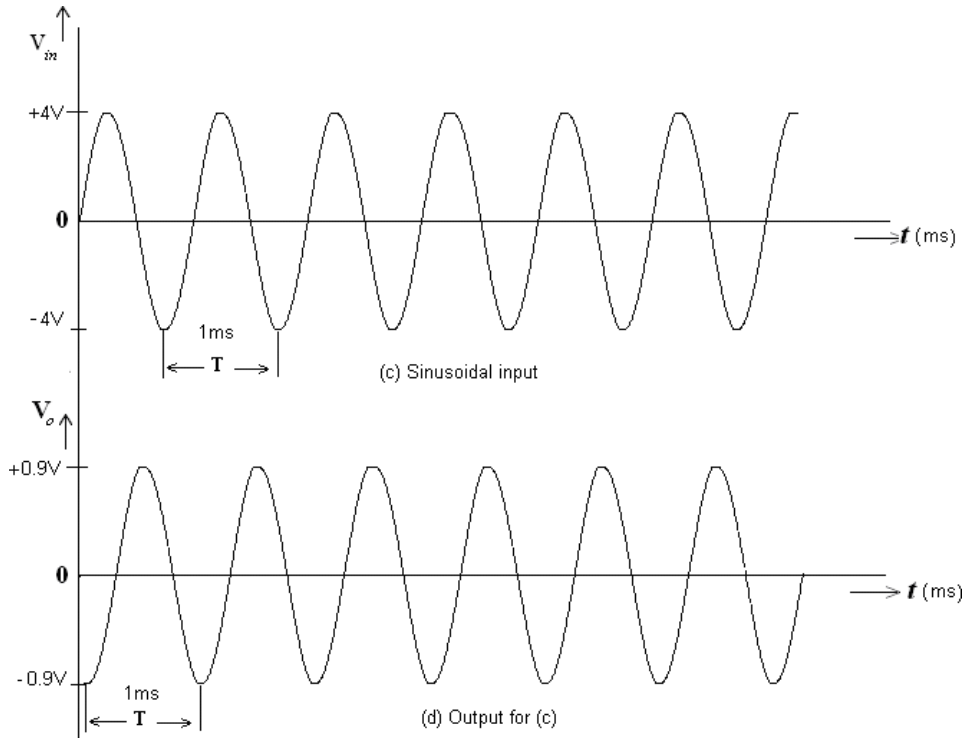
Wave Integrator:Fig7(a): Input and output waves forms of integrator





Differentiator:Fig7(b):Input and output waveforms of Differentiator





Sample readings:

Adder:

i/p_1(V)	i/p_2(V)	V_o(V)

Integrator:

Input–Square wave		Output-Triangular	
Amplitude(V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Input–sinewave		Output-cosine	
Amplitude(V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Differentiator:

Input–square wave		Output-Spikes	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Input–sinewave		Output-cosine	
Amplitude (V_{P-P}) (V)	Time period (ms)	Amplitude (V_{P-P}) (V)	Time period (ms)

Model Calculations: Adder

$V_o=-(i/p_1+i/p_2)$

If i/p_1= 2.5V and i/p_2= 2.5V, then

V_o= - (2.5+2.5) = -5V.

Integrator:

For T=1msec

$f_a=1/T=1KHz$

$f_a=1KHz=1/(2\pi R_f C_f)$

Assuming Cf= 0.1Kf, $R_f$is found from $R_f=1/(2\pi f_a C_f)$

$R_f=1.59\ K\Omega$

$R_f=10R_1$

$R_1=159\Omega$

Differentiator

For T=1msec

$f=1/T=1KHz$

$f_a=1KHz=1/(2\pi R_f C_1)$

Assuming C_1=0.1Kf,$R_f$is found from $R_f=1/(2\pi f_a C_1)$

$R_f=1.59K\Omega$

$f_b= 10\ f_a= 1/2\pi R_1 C_1$for

C_1= 0.1Kf;

$R_1=159\Omega$

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Result: For a given square wave and sine wave, output waveforms for integrator and differentiator are observed and the adder circuit is designed.

Inferences: Spikes and triangular waveforms can be obtained from a given square wave form by using differentiator and integrator respectively and the given signals can be added by using the adder circuit.

Viva Questions:

1. What are the applications of differentiator?
2. What are the applications of integrator?
3. What is a difference between inverting and non-inverting amplifier?

Subtractor

AIM : Todesignandsubtractorcircuitusing IC741andverifytheoutputsfor Different inputs.

Apparatus required:

Name of the Component/Equipment	Specifications	Quantity
Resistors	1KΩ	4
IC741	-	1
Cathode Ray Oscilloscope	20MHz	1
Multimeter	-	1
DualRegulatedpower supply	-	1

THEORY :

The CircuitwhichwillSubtracttheTwo inputs Voltages is called subtractoror differenceAmplifierCircuit.InordertofindtheRelationshipbetweenInputandoutputweneed to apply superposition theorem.

CIRCUITDIAGRAM:

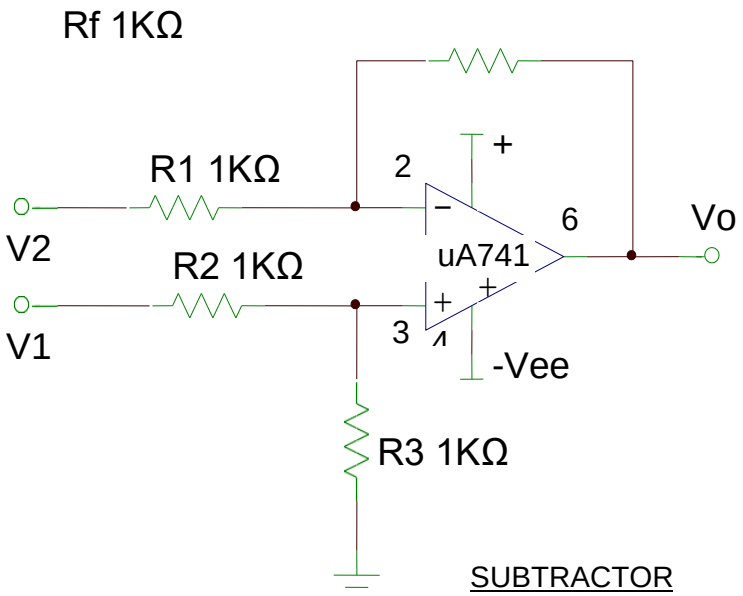


Fig. 7.4

By making V_2=0,The Circuit will become Non inverting Amplifier So

$$V_{01}=\left[1+\frac{Rf}{R1}\right]\left[\frac{Rf}{R2+Rf}\right]V_2.$$

Similarly by making V1=0, The Circuit will become Inverting Amplifier.

$$V_{02}=-(Rf / R1)\ V_1.$$

As $V_o=V_{o1}+V_{o2}$

The total Output of the Difference Amplifier is

$$V_o=\frac{Rf}{R1}(V_1-V_2)$$

$R_1=R_2=R_3=R_F=R$, Then

$V_O= V_1– V_2$.

PROCEDURE:

1. Connected the circuit as shown in the diagram
2. Switched ON the DC supply and adjusted +Vcc=15V and–V_{EE}=15V
3. For various values of V_1,V_2,and checked V_0 and verified whether $V_0$is,(V_1- V_2) or not.

Sample readings:

SUBTRACTOR:

i/p_1(V)	i/p_2(V)	V_o(V)

Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

RESULT:

For a given Subtractor Circuit Using IC741Verified the Outputs for Different Inputs.

Viva Questions:

1. What are the applications of op-amp?
2. What is a difference between inverting and non-inverting amplifier?

8.Instrumentation Amplifier using op-Amp

AIM: To study the operation of instrumentation Amplifier

Apparatus:

- IC-741op-Amps-3
- Resistors10KΩ-4
- Multimeters-2
- Regulated power supply(0-30)V,1A-2

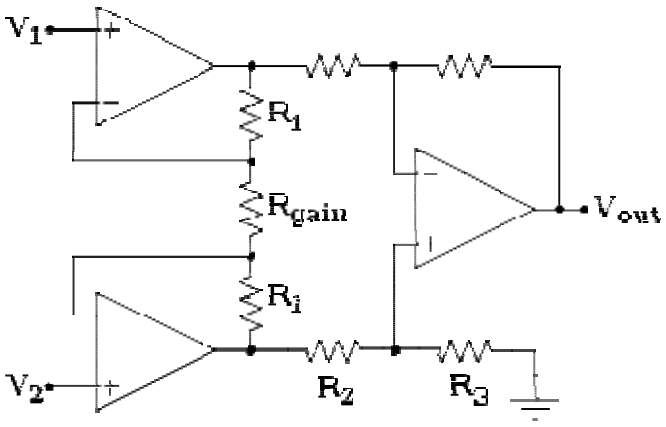


Fig8.1:Instrumentation Amplifier

Procedure:

1. Set up the circuit shown in fig8.1
2. Calculate the output voltage "V_{out}"
3. Calculate the V_{out} where $V_{out}=(V_2-V_1)(1+2R_1/R_{gain})(R_3/R_2)$
4. Compare it with practical output voltage.

5. Important features of Instrumentation amplifier:

- High gain accuracy
- High CMRR
- Low dc-offset
- Low output impedance

Applications:

Measurement & control of temperature, humidity light intensity, waler flow...etc.

Precautions:

1. Loose connections should be avoided
2. Positive and Negative supplies should be given correctly to IC741
3. Waveforms should be taken in accordance with the scale
4. High gain stability with low-temperature Co-efficient

Viva Questions:

1) What is CMRR?
2) What is characteristic of Ideal OPAMP?
3) Which OPAMP don't have feedback loop?

9.WAVE FORM GENERATION USINGOP-AMP (SQUARE&TRIANGULAR)

Aim: To generate square wave and Triangular wave form by using OPAMPs.

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	741IC	Refer AppendixA	2
2	Capacitors	0.01µf	2
3	Resistors	10kΩ 100kΩ	1 5
4	Regulated Power supply	(0–30V),1A	1
5	Cathode Ray Oscilloscope	(0-20MHz)	1

Theory: Function generator generates waveforms such as sine, triangular, square waves and so on of different frequencies and amplitudes. The circuit shown in Fig1 is a simple circuit which generates square waves and triangular waves simultaneously. Here the first section is a square wave generator and second section is an integrator. When square wave is given as input to integrator it produces triangular wave.

Circuit Diagram:

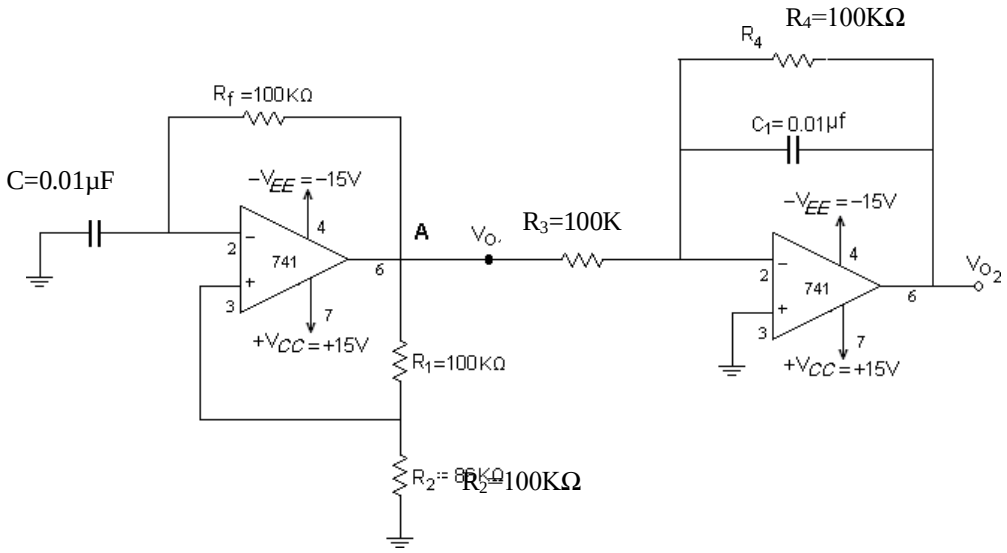


Fig9.1 Waveform Generation

Design:

Square wave Generator:

$T=2R_fCln(2R_2+R_1/R_1)$

Assume R_1= 1.16

R_2Then $T= 2R_fC$

Assume C and find

R_fAssume $R_1$and find R_2

Integrator:

Take $R_3C_f>>T$

$R_3C_f=10T$

Assume $C_f$find

R_3Take $R_3C_f= 10T$

Assume C_f= 0.01Kf

R_3= 10T/C

=20KΩ

Procedure:

1. Connect the circuit as per the circuit diagram shown in Fig9.1.
2. Obtain square wave at A and Triangular wave at V_o as shown in below figs.
3. Draw the output wave forms as shown in below figs.

Model Calculations:

For T=2msecT

$=2R_fC$

Assuming $C=0.1KfR_f$

$=2.10^{-3}/2.01.10^{-6}$

$=10K\Omega$

Assuming $R_1=100KR_2$

$=86K\Omega$

Sample readings:

Square Wave:V_{p-p}

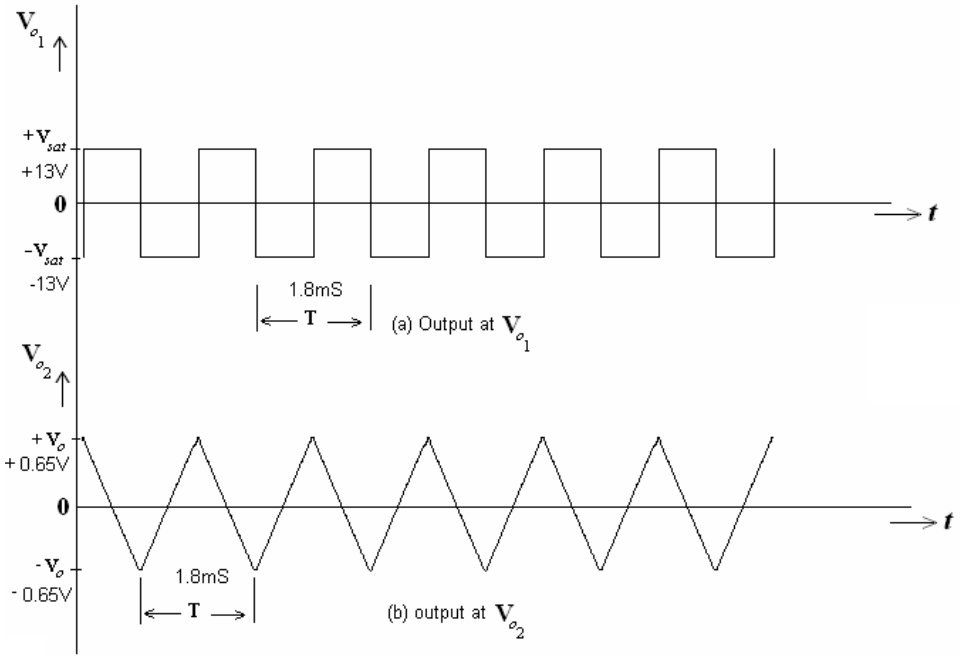
=26V(p-p)T=1.8

msec Triangular

Wave: V_{p-p}= 1.3V T=

1.8 msec

Wave Forms:



Precautions: Check the connections before giving the power supply.

Readings should be taken carefully.

Result: Square wave and triangular wave are generated and the output wave forms are observed.

Inferences: Various waveforms can be generated

Viva Questions:

1.Draw the characteristics of ideal comparator and that of a commercially available comparator

2. What are the other applications of op-amp
3. List the different types of comparator
4. What is meaning of voltage limiting?Show how it is obtained?

10.Design of Active Filters–LPF,HPF(First Order)

Aim: To design and obtain the frequency response of

i) First order Low Pass Filter(LPF)

ii) First order High Pass Filter(HPF)

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	IC741	Refer AppendixA	1
2	Resistors	10kΩ	3
3	capacitors	0.01µf	1
4	Cathode Ray Oscilloscope	(0–20MHz)	1
5	RPS	(0–30V),1A	1
6	Function Generator	(1Hz–1MHz)	1

Theory:

a) LPF:

A LPF allows frequencies from 0 to higher cutoff frequency, f_H.At f_H the gain is $0.707A_{max}$,and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is20dB/decade or6dB/octave, where octave signifies a twofold increase in frequency. The frequency $f=f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are-3dB frequency, break frequency, or corner frequency.

b) HPF:

The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called “low cut off frequency”. Obviously, all frequencies higher than $f_L$are pass band frequencies with the highest frequency determined by the closed – loop band width all of the op-amp.

Circuit diagrams:

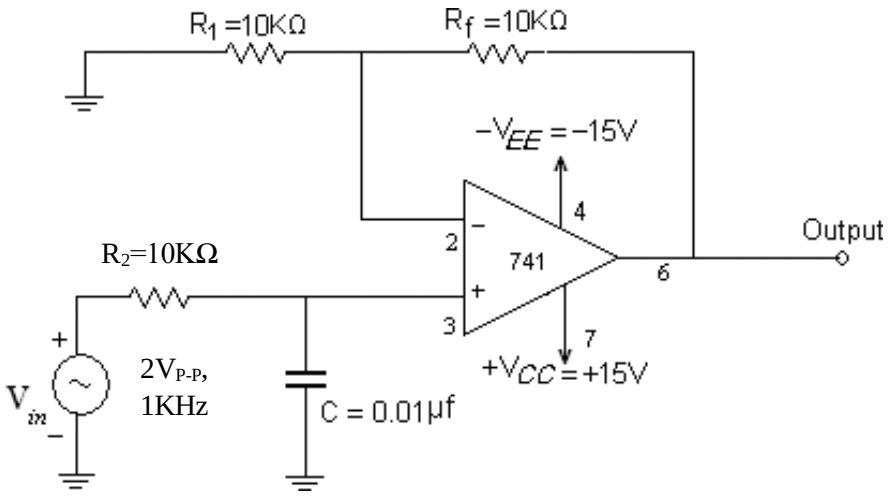


Fig10.1:Active Low pass filter

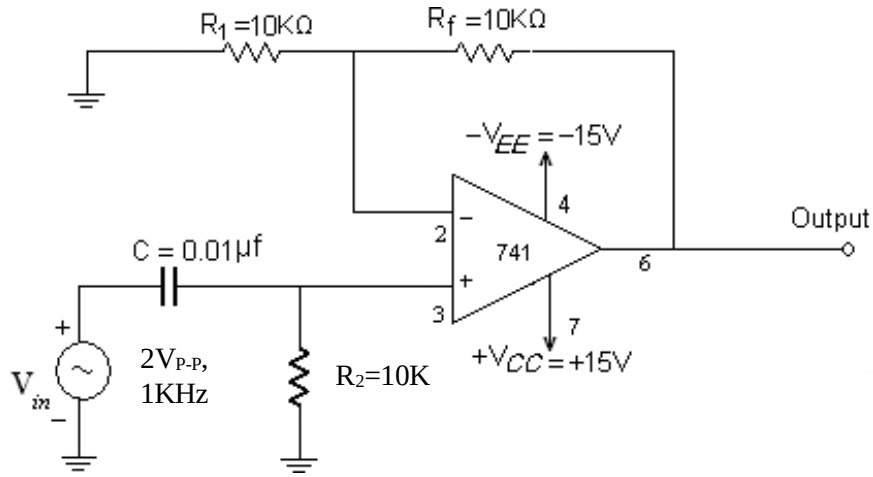


Fig10.2:Active High pass filter

Design:

First Order LPF: To design a Low Pass Filter for higher cutoff frequency f_H=4KHz and pass band gain of 2

$f_H=1/(2\pi RC)$

Assuming C=0.01μF,the value of R is found from $R= 1/(2\pi f_H C)\ \Omega = 3.97K\Omega$

The pass band gain of LPF is given by $A_F= 1+ (R_F/R_1)=2$ Assuming $R_1=10K\Omega$,the value of R_F is found from

$R_F=(A_F-1)R_1=10K\Omega$

First Order HPF: To design a High Pass Filter for lower cutoff frequency f_L=4 KHz and pass band gain of 2

$f_L= 1/(2\pi RC)$

Assuming C=0.01μF,the value of R is found from $R= 1/(2\pi f_L C)\ \Omega = 3.97K\Omega$

The pass band gain of HPF is given by

$A_F=1+ (R_F/R_1)=2$ Assuming $R_1=10\ K\Omega$, the value of $R_F$is found from

$R_F=(A_F-1)R_1=10K\Omega$

Procedure:

First Order LPF:

1. Connections are made as per the circuit diagram.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and noted own the output amplitude at each step as shown in Table (a).
4. Plot the frequency response.

First Order HPF:

1. Connections are made as per the circuit diagrams.
2. Apply sinusoidal wave of constant amplitude as the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table (b).
4. Plot the frequency response as shown in fig

Tabular Form and Sampled Values:

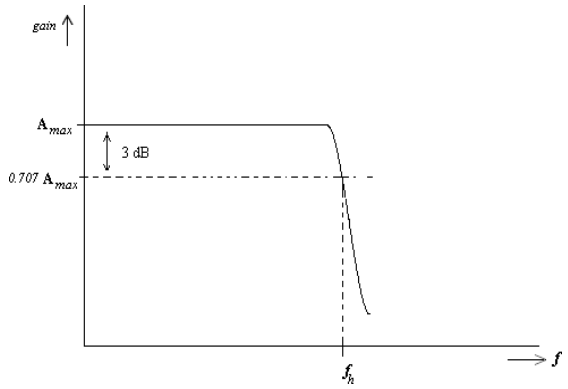
a) LPF b) HPF

Input voltage V_{in}=0.5V

Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain in dB

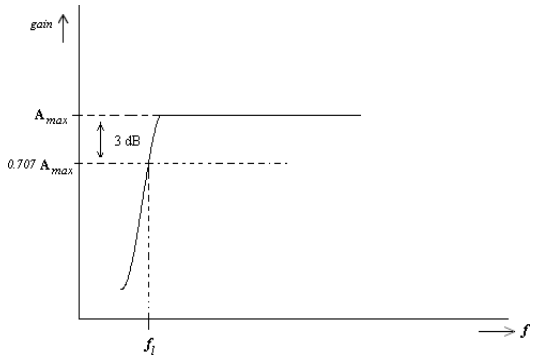
Frequency	O/P Voltage(V)	Voltage Gain Vo/Vi	Gain in dB

Model graphs:



Fig(a)

Frequency response characteristics of LPF



Fig(b)

Frequency response characteristics of HPF

Precautions:

- Check the connections before giving the power supply.
- Readings should be taken carefully.
- V_{CC} and V_{EE} must be given to the corresponding pins.

Result: First order low-pass filter and high-pass filter are designed and frequency response characteristics are obtained.

Inferences: By interchanging R and C in a low-pass filter, a high-pass filter can be obtained.

Viva Questions:

1. What is filter?
2. What is an active filter?
3. What is high pass filters & low pass filters?
4. Name the types of filters?
5. What is butter worth filter?

11.APPLICATIONS OF IC555 TIMER

(Monostable &AstableMultivibrators , Schmitt trigger)

(A) Monostable &Astable Multivibrators

Aim: To generate a pulse using monostable multivibrator and to generate unsymmetrical square and symmetrical square waveforms using IC555

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC555	Refer AppendixB	1
2	Resistors Resistor	2.2kΩ,3.3kΩ 100kΩ	Each one 1
3	Capacitors	0.1µf,0.01µf	Each one
4	Regulated Power supply	(0–30V),1A	1
5	Cathode Ray Oscilloscope	(0–20MHz)	1

Theory:

Monostable operation:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In Astable or standby mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high (□VCC). The time the output remains high is determined by the external RC network connected to the timer.At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low),hence the name monostable. Normally the output of the Monostable Multivibrator is low.

When the power supply VCC is connected, the external timing capacitor 'C" charges towards VCCWith a time constant(RA+RB)C.Duringthistime,pin3ishigh(≈VCC) as Reset R=0,Set S=1 and this combination makes Q =0 which has unclamped the timing capacitor 'C'. For pin configuration and specifications, see Appendix-C

Astable operation:

When the capacitor voltage equals 2/3 VCC, the UC triggers the control flip flop on that$Q$=1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through RBand transistor Q1 with a time constant RBC. Current also flows into Q1 through RA. Resistors RAand RBmust be large enough to limit this current and prevent damage to the discharge transistorQ1.

The minimum value of RAis approximately equal to VCC/0.2 where 0.2A is the maximum current through the ON transistor Q1.

During the discharge of the timing capacitor C, as it reaches VCC/3, the LC is triggered and at this stage S=1, R=0 which turns $\overline{Q}$=0. Now Q=0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 VCCand 1/3VCCrespectively. The length of time that the output remains HIGH is the time for the Capacitor to charge from1/3VCCto2/3VCC.

The capacitor voltage for a low pass RC circuit subjected to a step input of VCC Volts is given by $V_C = V_{CC}(1-e^{-t/RC})$

Total time period T= 0.69 (RA+ 2RB)C

f=1/T=1.44/(RA+2RB)

Circuit Diagrams:

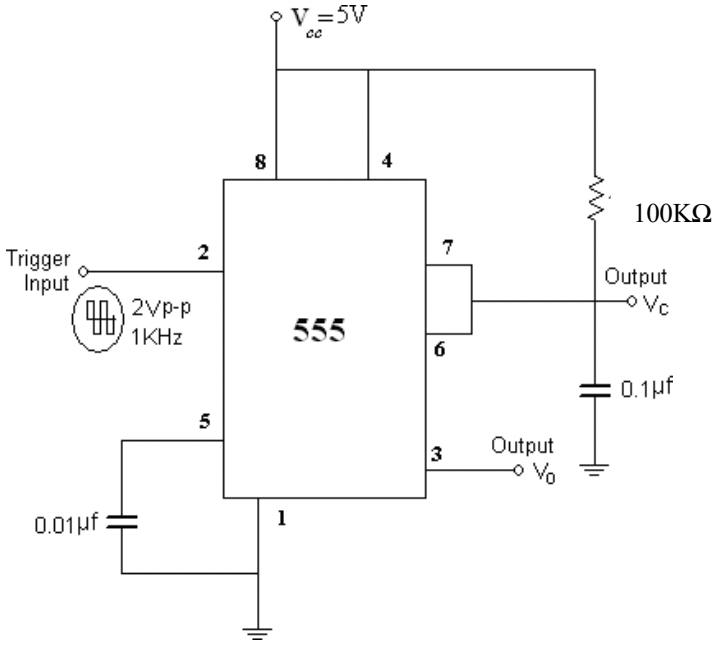


Fig11.1:Monostableoperation

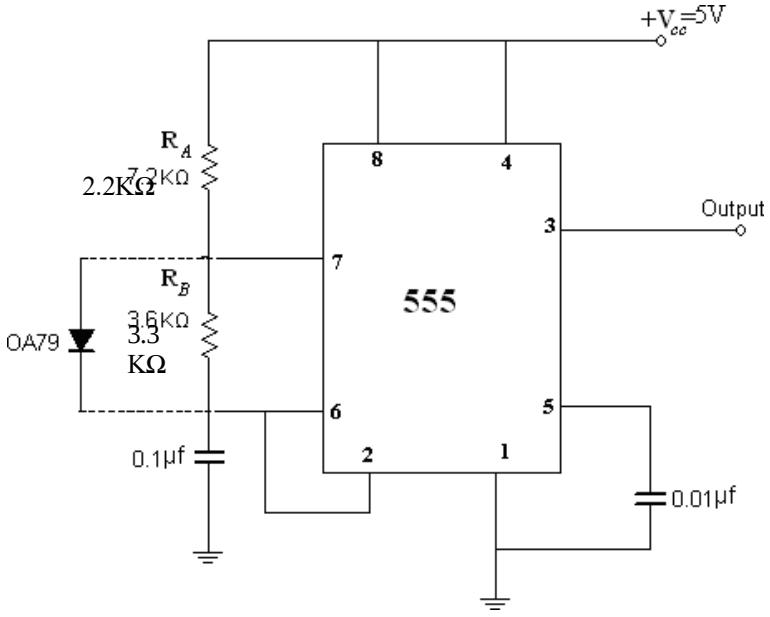


Fig11.2:Astable operation

Design:

Monostable operation:

Consider V_{CC}=5V,for given t_p

Output pulse width t_p=1.1R_AC

Assume C in the order of microfarads & Find R_A

Astable operation:

Formulae:f=1/T=1.44/(R_A+2R_B)C

Duty cycle, D=t_c/T=R_A+R_B/(R_A+2R_B)

Model calculations:

Monostable operation:

If C=0.1 µF, R_A= 10k then t_p= 1.1 m Sec

Trigger Voltage =4 V

Astable operation:

Given f=1KHzandc=0.1KF,D=0.25

$\therefore$1KHz=1.44/(RA+2R_B)x0.1x10^{-6}and0.25=R_A+R_B/R_A+2R_B

Solving both the above equations, we obtain R_A & R_B as R_A= .2KΩ

R_B= 3.6KΩ

Procedure:

Monostable operation:

1. Connect the circuit as shown in the circuit diagram as shown in Fig11.1.
2. Apply Negative triggering pulses at pin2 of frequency 1KHz.
3. Observe the output waveform and capacitor voltage and measure the pulse duration
4. Theoretically calculate the pulse duration as T_{high}=1.1.R_aC
5. Compare it with experimental values.

Astable operation:

I) Unsymmetrical Square wave

1. Connect the circuit as per the circuit diagram shown in Fig 11.2 without connecting the diode OA 79.
2. Observe and note down the output waveform at pin3 and across timing capacitor.
3. Measure the frequency of oscillations and duty cycle and then compare with the given values.
4. Sketch both the waveforms to the same time scale.

II) Symmetrical square wave form generator:

1. Connect the diode OA79 as shown in fig(ii)to get D=0.5or50%.
2. Choose R_a=R_b=10KΩ and C=0.1μF
3. Observe the o/p wave form,measure frequency of oscillations and the duty cycle and then sketch the o/p waveform.

Waveforms:

Monostable operation:

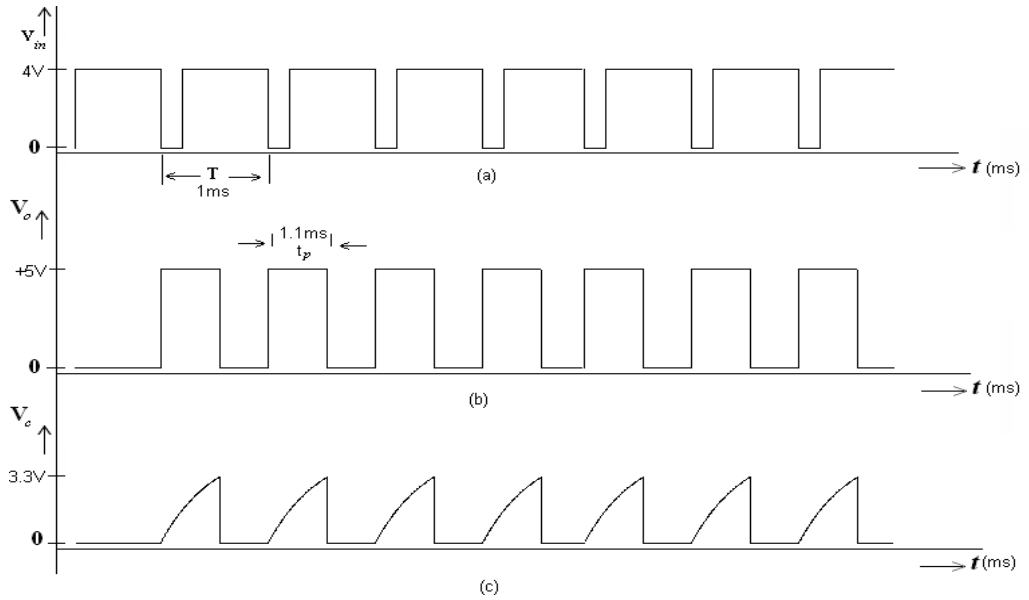


Fig 11.I (a): Trigger signal (b): Output Voltage(c):Capacitor Voltage

Astable operation:

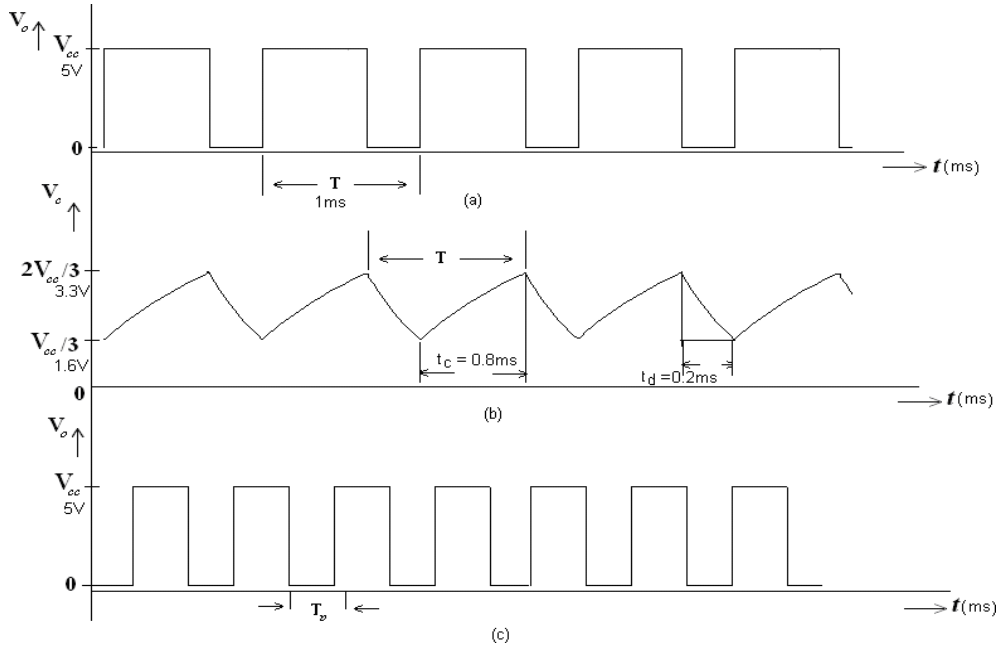


Fig 11.II (a): Unsymmetrical square wave output

(b):Capacitor voltage of Unsymmetrical square wave

Output(c):Symmetrical square wave output

Sample Readings:

Monostable operation:

Trigger	Output wave	Capacitor output
0to5V range 1)1V,0.09msec	0to5V range 4.6V,0.5msec	0to3.33Vrange 3V,0.88msec

Astable operation:

	Unsymmetrical	Symmetrical
Voltage V_{PP}	≈5V	≈5V
Time Period	0.1msas T_C=0.08ms T_D=0.02ms	0.1msas T_C=0.05ms T_D=0.05ms
Duty cycle	80%	50%

Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

The input and output waveforms of 555 timer monostable multivibrator are observed.

Both unsymmetrical and symmetrical square waveforms are obtained and time period at the output is calculated in astable mode.

Inferences:

Output pulse width depends only on external components R_A and C connected to IC555.Unsymmetrical square wave of required duty cycle and symmetrical square waveform Can be generated.

Viva Questions:

1. Define Duty Cycle?
2. What are the other applications of 555 timer?
3. Draw the internal circuit diagram of 555 timer?
4. Explain the operation of 555 timer?

(B) Schmitt TriggerCircuit– using IC555

Aim: ToconstructandstudytheSchmittTriggerusingIC555OperationalAmplifiers

Apparatus Required:

1. Function Generator
2. Regulated DC power Supply
3. Dual Channel Oscilloscope(CRO)
4. Digital Multimeter

S. No	Name of the Component	Quntity (in No's)
1	IC 555	1
2	Resistors (100K)	2
3	Capacitor (0.1uf)	1
	Capacitor (0.01uf)	1

Circuit diagram:

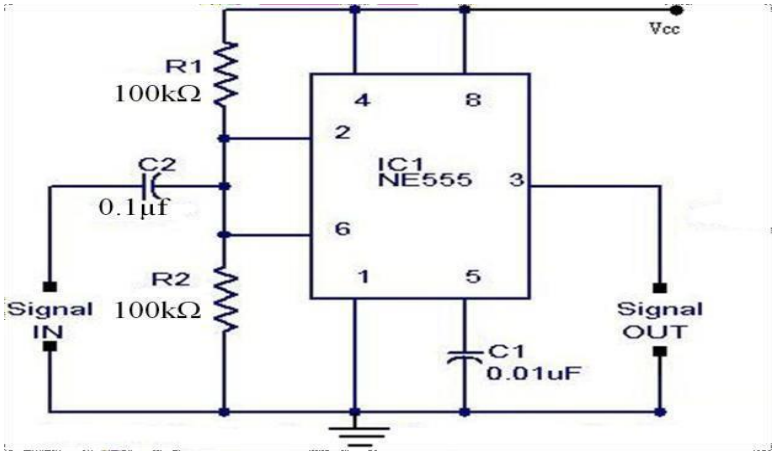


Fig 11.3:circuit diagram of Schmitt trigger using IC 555

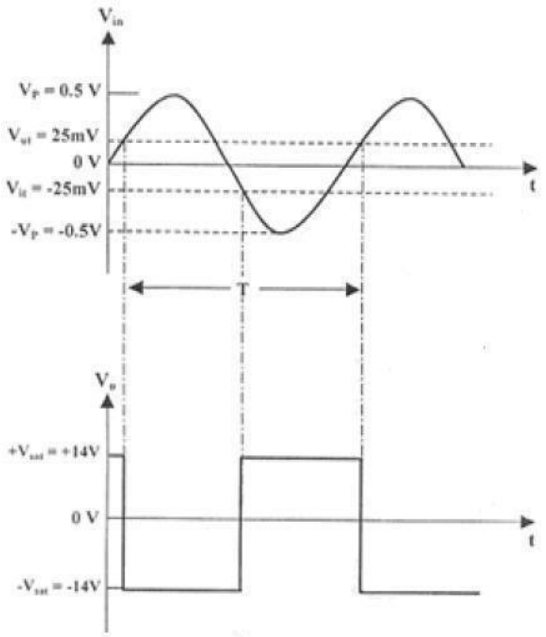
Theory:

In Schmitt Trigger two internal comparators are tied together and externally biasedat VCC/2 through R1& R2. Since the upper comparator will trip at (2/3) VCC and lowercomparator at (2/3) VCC the bias provided by R1 & R2is centered within these two thresholds. Thus a sine wave of sufficient amplitude (>VCC/6=2/3VCCVCC/2) to exceed there reference levels causes the internal flip-flop to alternately set and reset providing a square wave output

Procedure for IC555:

1. Connect the circuit as shown in fig(10.2).
2. Apply the input sinewave 5V(P-P) using function generator at1KHZfrequency.
3. Observe the output wave format PinNo:3.

Input and Output Wave forms of Schmitt Trigger:



Observations for Schmitt trigger usingIC555:

Input signal
Amplitude= Time period=
Output signal
Amplitude= Time period=

Applications:

1. on/off controllers
2. Used as a comparator

Result: Hence constructed and studied Schmitt trigger usingIC555

Viva Questions:

1. What do mean by Schmitt trigger?
2. What are the different applications Schmitt triggers?
3. What is meant by Hysteresis voltage?
4. What is meant by threshold voltage?

12.PLL Using 1C565

Aim: To study the operation of PLL using NE/SE 565.

Apparatus:

- 1C chip NE/SE565.
- CRO.
- Signal generator
- 0.001U.F,1uF capacitors.
- 6.8KΩ resistor

Theory:

The 565 IC is available as a14-pin DIP package. The output frequency of the VCO is fo = 1.2 /4 RTCT, where RT and CT are the external Resistor and Capacitor connected to pin 8 and pin 9. A value between 2k and 20k is recommended for RT. The VCO free running frequency is adjusted with RT and CT, so that it is at the center of the input frequency range.

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

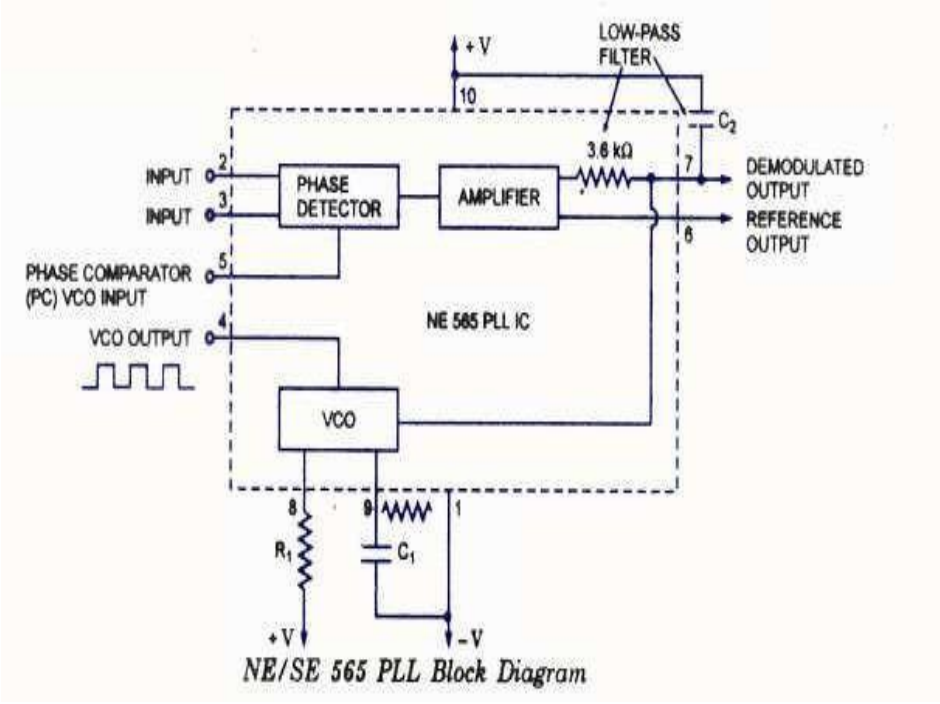
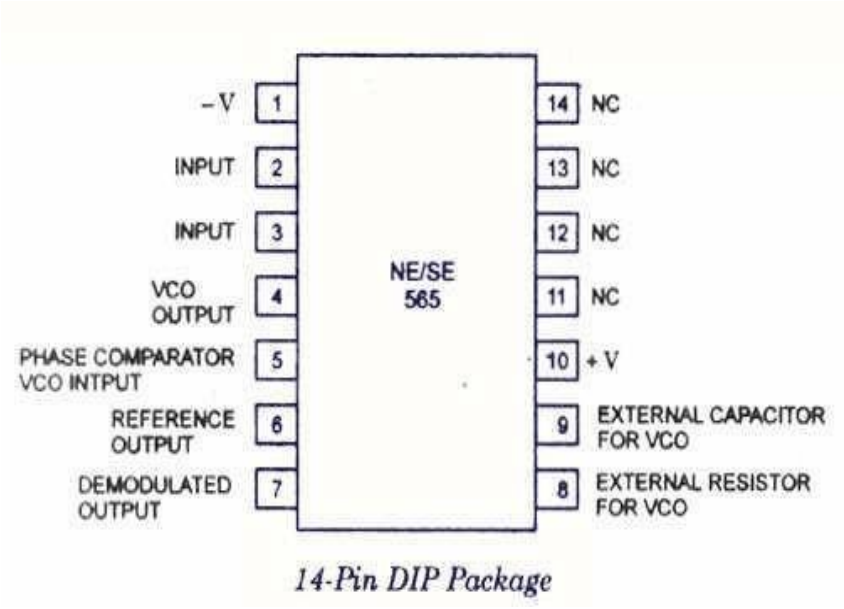


Fig12.1

Pin diagram for 1C chip NE/SE565



14-Pin DIP Package

PLL applications:

1. Frequency multiplication/division
2. Frequency translation.
3. AM detection.
4. FM demodulation
5. FSK demodulator.

Procedure:

1. Make connections of the PLL as shown in fig
2. Measure the free running frequency of "VCO at pin4. With the i/p signal V_{in}, set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$
3. Now apply thei/p signalof1 V_{PP}, square wave at a1 KHz to pin2.connect one channel of the scope to pin2 and display this signal on the scope.
4. Gradually increase thei/p frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing thei/p frequency, till PLL tracks the i/p signal, say. to a frequency "f_2". This frequency "f_2"gives the upper end of the lock range.Ifi/p frequency is increased further, the

loop will get unlocked.

5. Now gradually decrease the i/p frequency till the PLL is again locked. This is the frequency (f3) the upper end of the capture range. Keep on decreasing the i/p frequency until the loop is unlocked. This frequency 'f_4'gives lower end of lock range.
6. The lock range $\Delta f_L=f_2-f_4$. Compare it with the calculated value of$\pm 7.8f_o/12$.Also the capture range is $\Delta f_c=(f_3-f_1)$.Compare it with the calculated value of capture range.

Result:

Theoretical values of lock range, capture range, free running frequency are obtained.

Viva Questions:

1.What are the basic blocks of a PLL?

2.What are the applications of PLL?

3.Define V_{CO}?

4.What is the formula for the free running frequency F_o of 565 PLL?

13.IC723 Voltage Regulator

Aim: To design a low voltage variable regulator of 2 to 7V using IC723.

Apparatus required:

S.No	Equipment/Component name	Specifications/Value	Quantity
1	IC723	Refer appendix A	1
2	Resistors	3.3KΩ,4.7KΩ, 100Ω	Each one
3	Variable Resistors	1KΩ,5.6KΩ	Each one
4	Regulated Power supply	0-30 V,1A	1

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages.

For a low voltage regulator, the output $V_O$can be varied in the range of voltages $V_o < V_{ref}$, whereas for high voltage regulator, it is $V_O > V_{ref}$. The voltage V_{ref} is generally about 7.5V. Although voltage regulators can be designed using Op-amps, it is quicker and easier to use IC voltage Regulators.

IC 723 is a general purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Further more it is an adjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode of operation. Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator. The pin configuration and specifications are shown in the Appendix-A.

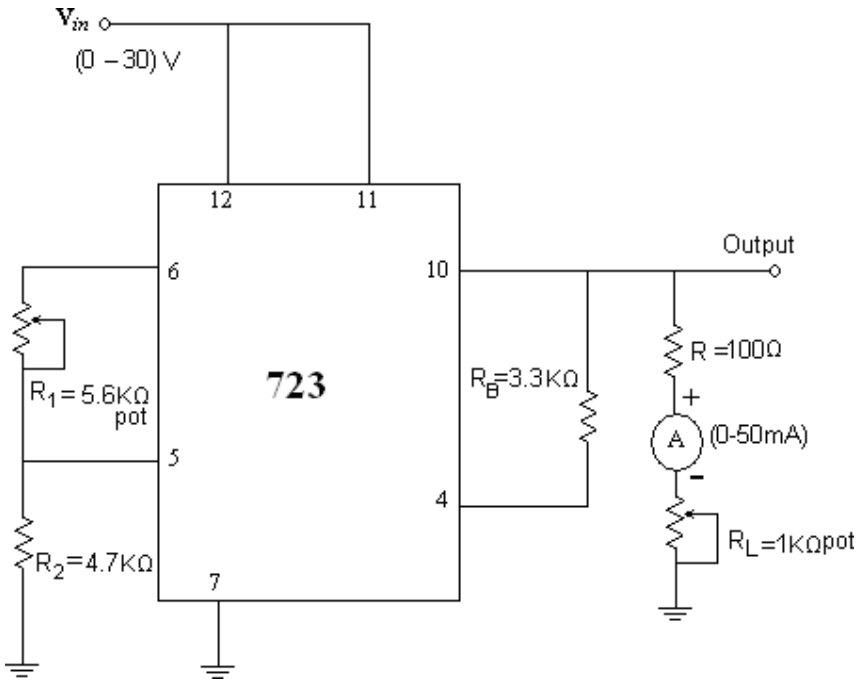


Fig 13.1:Voltage Regulator

Design of Low voltage Regulator:

Assume I_o=1mA,V_R=7.5VR_B=3.3KΩ

For given V_o

$R_1=(V_R–V_O)/I_o$

$R_2=V_O/I_o$

Procedure:

a) **Line Regulation*:***

1. Connect the circuit as shown in fig1.
2. Obtain $R_1$and R_2 for V_o=5V
3. By varying V_n from 2 to10V, measure the output voltage V_o.
4. Draw the graph between V_n and V_o as shown in model graph(a)
5. Repeat the above steps for V_o=3V

b) Load Regulation :For V_O=5V

1. Set $V_i$such that V_O=5V
2. By varying R_L, measure I_L and V_o
3. Plot the graph between I_L and V_o as shown in model graph(b)

4. Repeat above steps 1 to 3 for V_O=3V.

Sample Readings

a) Line Regulation:

V_o set to5V

Vi(V)	Vo(V)

Vo set to 3V

Vi(V)	Vo(V)

b) Load Regulation:

Vo set to 5V

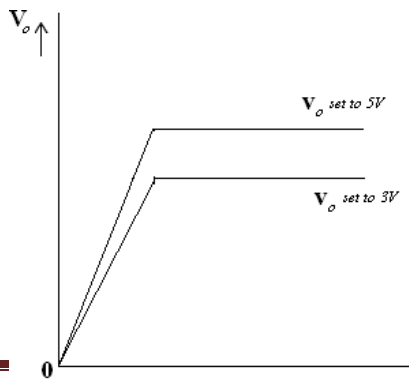
I_L(mA)	Vo(V)

Vo set to 3V

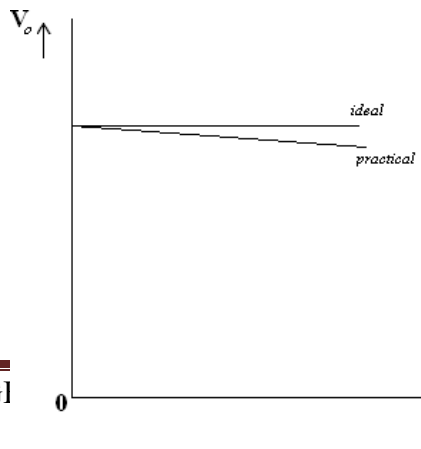
I_L(mA)	Vo(V)

Model waveforms:

a)LineRegulation



b)Load Regulation



Precautions:

Check the connections before giving the power supply.

Readings should be taken carefully.

Results:

Low voltage variable Regulator of 2V to 7V using IC 723 is designed. The line and load regulation characteristics are plotted.

Inferences:

Variable voltage regulators can be designed by using IC723.

Output varies linearly with input voltage up to some value(o/p voltage + dropout voltage) and remains constant.

Viva Questions:

1. What is meant by line regulation?
2. What is the function of a series pass transistor in Linear regulated power supply?
3. What is meant by current limiting?
4. What are the advantages of IC voltage regulators?

14. DESIGN OF VCO USING IC566

Aim: i) To observe the applications ofVCO-IC566

i) To generate the frequency modulated wave by using IC566

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	IC566	Refer pageno10	1
2	Resistors	10KΩ 1.5KΩ	2 1
3	Capacitors	0.1μF 100pF	1 1
4	Regulated power supply	0-30V, 1A	1
5	Cathode Ray Oscilloscope	0-20MHz	1
6	Function Generator	0.1-1MHz	1

Theory: The VCO is a free running Multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying ad. c control voltage $v_c$to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "voltage controlled oscillator" or, in short, VCO.

The output frequency of the VCO can be changed either by R_1, C_1or the voltage $V_C$at the modulating input terminal (pin 5). The voltage $V_C$can be varied by connecting a R_1R_2circuit. The components $R_1$and $C_1$are first selected so that VCO output frequency lies in thecentre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC}which can produce a frequency variation of about 10 to 1.

Circuit Diagram:

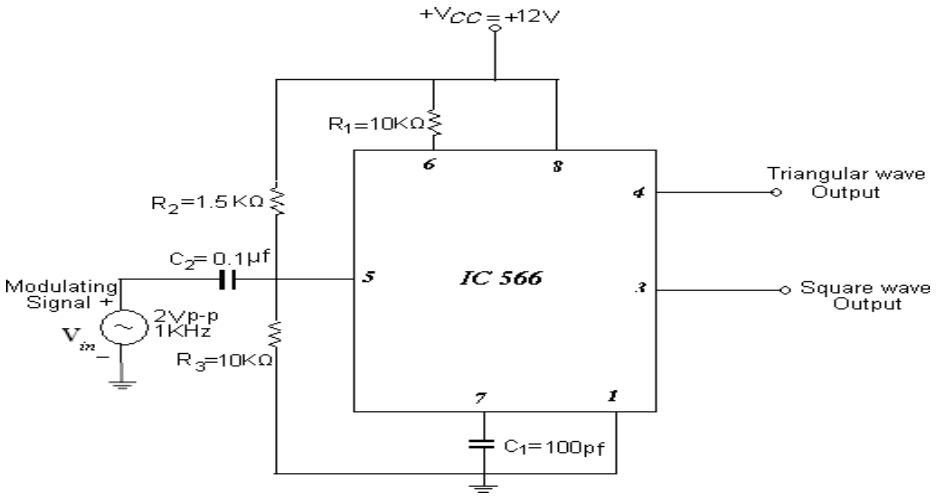


Fig 14.1:Voltage Controlled Oscillator

Design:

1. Maximum deviation time period=T.
2. $f_{min}=1/T$.
   where f_{min} can be obtained from the FM wave
3. Maximum deviation, $\Delta f=f_o-f_{min}$
4. Modulation index $\beta=\Delta f/f_m$
5. Bandwidth BW= $2(\beta+1)f_m=2(\Delta f+f_m)$
6. Free running frequency, $f_o=2(V_{CC}-V_c)/R_1C_1V_{CC}$

Procedure:

1. The circuit is connected as per the circuit diagram shown in Fig14.1.
2. Observe the modulating signal on CRO and measure the amplitude and frequency of the signal.
3. Without giving modulating signal, take output at pin4, we get the carrier wave.
4. Measure the maximum frequency deviation of each step and evaluate the modulating Index.

   $m_f= \beta= \Delta f/f_m$

Waveforms:

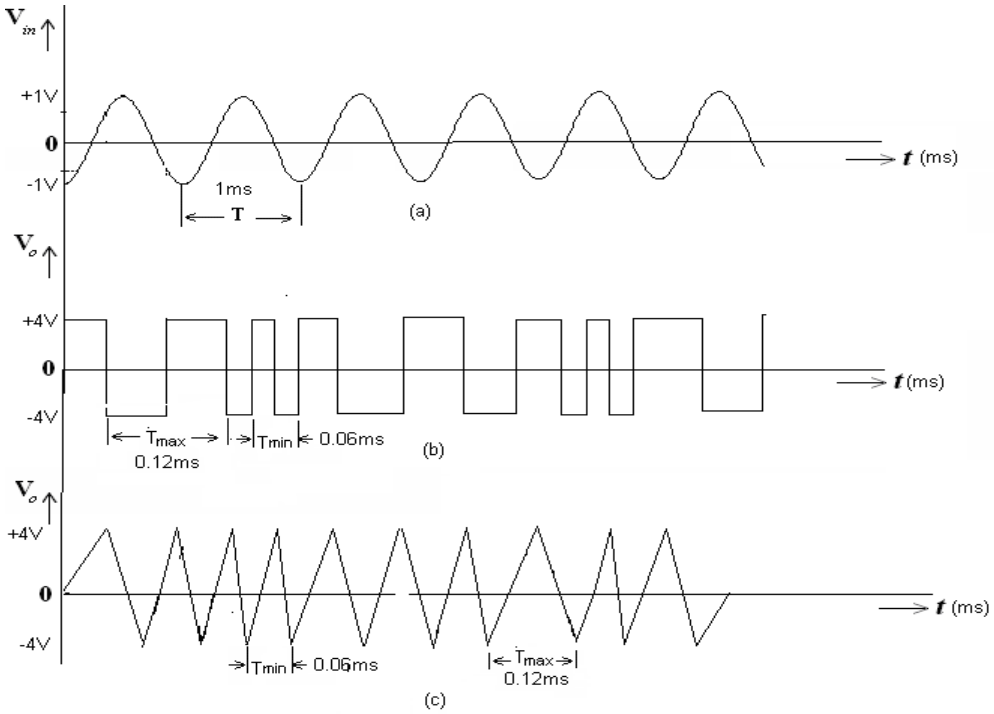


Fig 14(a):Input wave of VCO

(b): Output of VCO at pin3

(c): Output of VCO at pin

Sample readings:

V_{CC}=+12V;R_1=R_3=10KΩ;R_2=1.5KΩ;f_m=1KHz

Free running frequency, f_o=26.1KHzf_{min}=8.33KHz

Δf=17.77KHz

β=Δf/f_m=17.77

Band width BW≈ 36KHz

Precautions:

Check the connections before giving the power supply. Readings should be taken carefully.

Result:

Frequency modulated waveforms are observed and modulation Index ,B.W required for FM is calculated for different amplitudes of the message signal.

Inferences:

During positive half-cycle of the sine wave input, the control voltage will increase, the frequency of the output waveform will decrease and time period will increase. Exactly opposite action will take place during the negative half-cycle of the input as shown in Fig 14.(b).

Viva Questions:

1. What is the operation of IC 566 VCO?
2. What is the use of VCO?
3. What are the applications for VCO?
4. Which filter is used in VCO?

15.4 bit DAC using OPAMP

Aim: To designR-2R ladder Network DAC

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	741IC	Referpageno2	1
2	Resistors	1KΩ,2KΩ,4KΩ, 8KΩ	Each one
3	Regulated Power supply	(0-30)V, 1A	1
4	Multimeter (DMM)		1
5	Digital trainer Board		1

Theory: Digital systems are used in ever more applications, because of their increasingly efficient, reliable, and economical operation with the development of the microprocessor, data processing has become an integral part of various systems Data processing involves transfer of data to and from the microcomputer via input/output devices. Since digital systems such as microcomputers use a binary system of ones and zeros, the data to be put into the microcomputer must be converted from analog to digital form. On the other hand, a digital-to-analog converter is used when a binary output from a digital system must be converted to some equivalent analog voltage or current. The function of DAC is exactly opposite to that of an ADC.

A DAC in its simplest form uses an op-amp and either binary weighted resistors or R- 2R ladder resistors. In binary-weighted resistor op-amp is connected in the inverting mode, it can also be connected in the non-inverting mode. Since the number of inputs used is four, the converter is called a 4-bit binary digital converter.

Circuit Diagrams:

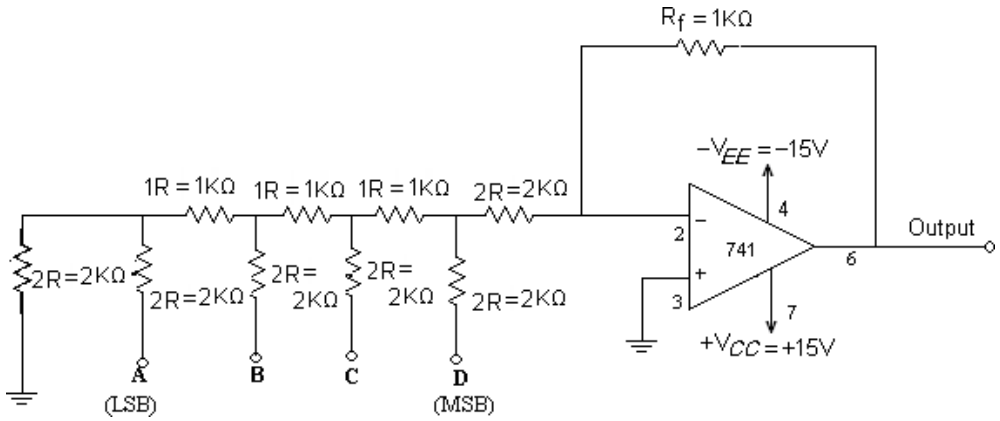


Fig 15.1: R–2R Ladder DAC

Output Voltage is given by

$$\mathbf{Vo = - V_R * (Rf / 2R) * (d1/2 + d2/4 + d3/8 + d4/16)}$$

where, V_R = 5V , Rf = 2R , d1 (MSB bit) and d4 (LSB bit)

Procedure:

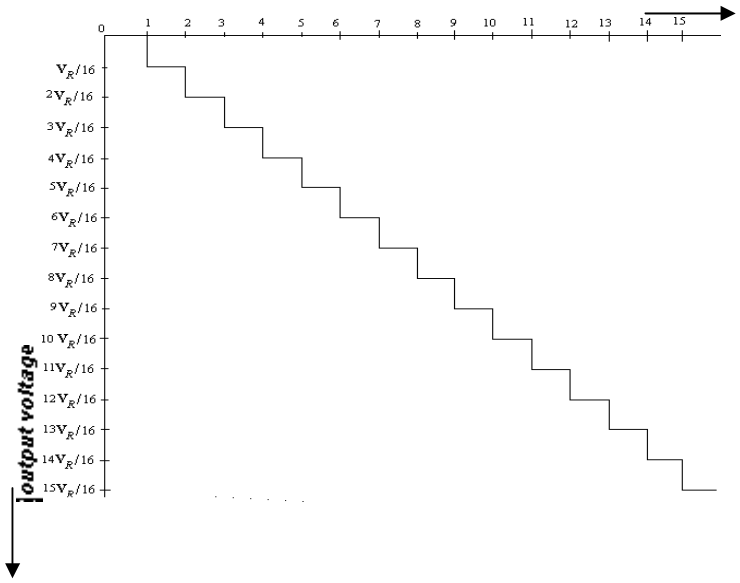
1. Connect the circuit as shown in Fig15.1.
2. Vary the inputs A,B,C,D from the digital trainer board and note down the output at pin 6. For logic '1', 5 V is applied and for logic '0', 0 V is applied.
3. Repeat the above two steps for R–2R ladder DAC shown in Fig15.2.

Observations:

R-2RLadderNetwork:

S.No	D	C	B	A	Theoretical Voltage(V)	Practical Voltage(V)

Model Graph: *Decimal Equivalent of Binary inputs*



Precautions:

Check the connections before giving the power supply. Readings should be taken carefully.

Results:

Outputs of R-2R ladder DAC are observed.

Viva Questions:

1. How does a 4-bit DAC work?
2. Why op amp is used in DAC?
3. What are the applications of DAC?
4. Which amplifier is used in DAC?

EXPERIMNT(S) BEYOND THE SYLLABUS

1. SAMPLING GATES

Aim:

To construct and verify the Sampling Gates and its output waveform.

Apparatus required:

S.No	Equipment/Component Name	Specifications/Value	Quantity
1	Diode	1N4007	1
2	Capacitor	0.01μF	1
3	Resistors	1KΩ	2
4	Function generator	-	1

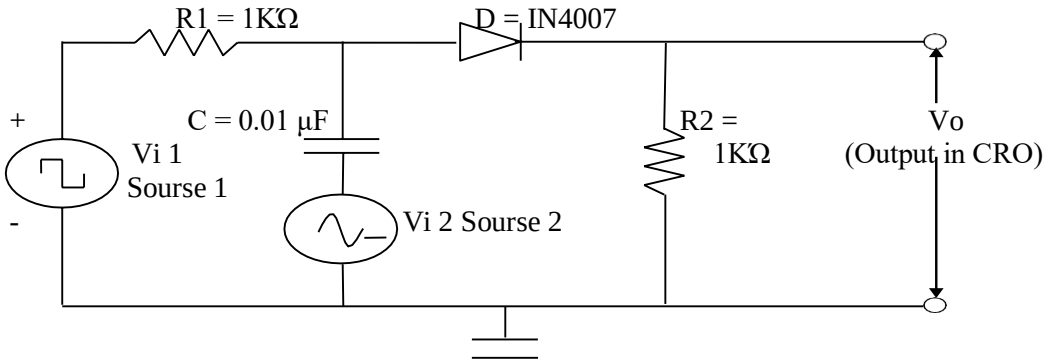
Theory:

A Sampling gate is basically a transmission circuit, which allows an input signal to pass through it during a selected interval and block its passage outside this time interval. A sampling gate is sometimes referred to as time-selection gates.

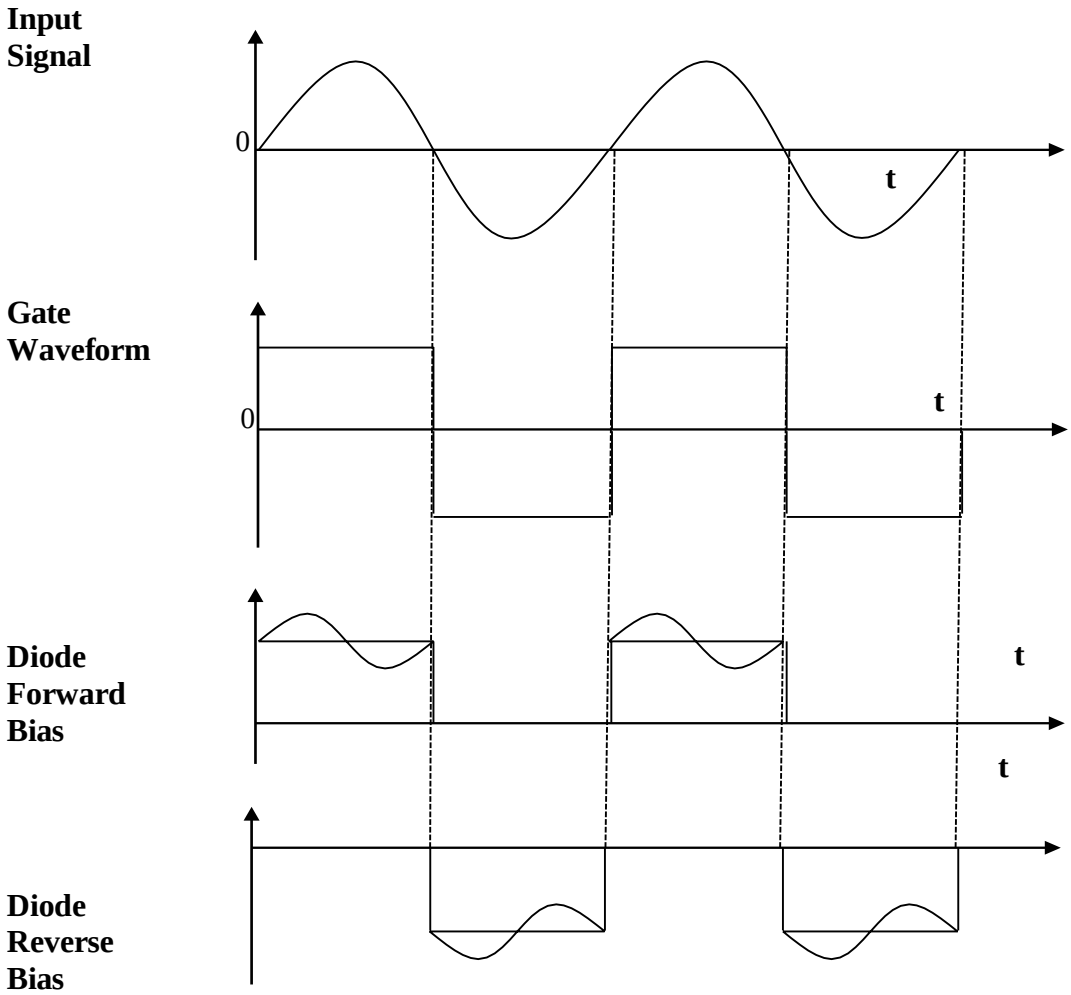
The circuit uses a diode D, with certain polarity, a capacitor C and resistors $R_1$and R_L. Capacitor $C_1$and $R_1$from together an integrating circuit, with the voltage levels $V_1$and $V_2$the diode gets heavily reverse biased respectively.

With the diode reverse biased, there is no conduction and hence the output is zero. This is equivalent to the open switch. When the gate voltage rises abruptly from $V_1$to V_2, the positive going input signal causes the diode to be forward biased. The diode conducts and the input voltage across R_L. If the conditions are assumed to be ideal, then there is neither attenuation nor distortion of the input signal. The output voltage would be an exact replica of the input signal.

Circuit diagram:



Model graph:



Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Thesquarewavesignalof4 volts is to be applied at the resistor R_1.
3. The another signal of sinewave signal of 4volts is to be applied at the capacitor C.
3. Obtain the output wave forms for the given input signals across the resistor R_2 from the CRO and the graph was plotted.

Result:

The Sampling Gates was constructed and the output wave forms are verified.

Viva-Voce Questions:

1. What is the principle of sampling gate?
2. What is a sampling gate also known as?
3. What is application of sampling gate?
4. What is the basic theory of sampling?

APPENDIX–A

BC107

Specifications:

1. Type	:Si–NPN
2.operatingpointtemp	:65^{o}to200^{o}C
3.I_C(max)	:100mA
4.h_{fe}(min)=110	:100
5.h_{fe}(max)	:450
6.V_{CE}(max)	:45V
7.P_{tot}(max)	:300mW
8.Category(typicaluse)	:Audio,low power
1. Possible substitutes	:BC182,BC547

Diode

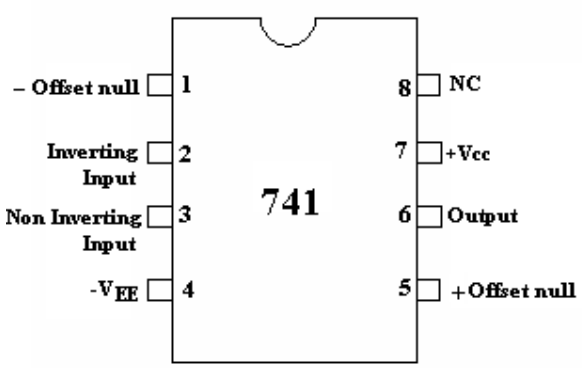
TypeNo	1N4007
Max.PeakInverseVolts	50
MaxRMSSupply Volts	35
MaximumForwardVoltage @ 1Ampere, DC @ 75^0 C	1.1Volts,Peak
MaximumReverseDCCurrent @PIV @ 25^0 C	10µA

MaximumDynamicReverseCurrent @PIV @75^0 C	30µA,Average

APPENDIX–B

IC741

Pin Configuration:



Specifications:

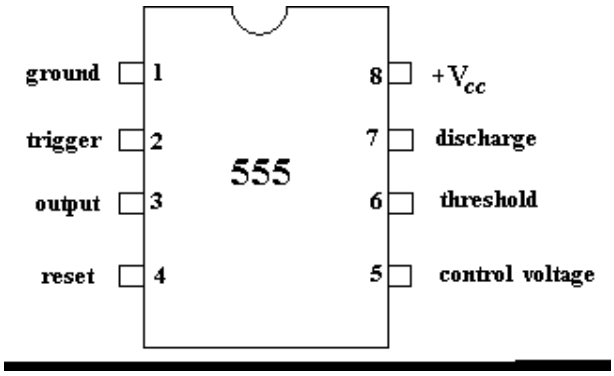
1. VoltagegainA=αtypically2,00,000
2. I/PresistanceRL=αΩ,practically2MΩ
3. O/PresistanceR1=0,practically75Ω
4. Bandwidth=αHz.Itcan beoperatedatanyfrequency
5. Common mode rejection ratio = α (Abilityofopamptorejectnoisevoltage)
6. Slewrate+αV/µsec (Rateofchange ofO/Pvoltage)
7. WhenV1=V2,VD=0
8. Inputoffsetvoltage(Rs≤10KΩ)max6mv
9. Inputoffsetcurrent=max200nA
10. Inputbiascurrent:500nA
11. Inputcapacitance:typevalue1.4PF
12. Offsetvoltageadjustmentrange:±15mV
13. Inputvoltagerange:±13V

14. Supplyvoltagerejectionratio:150μr/V
15. Outputvoltageswing:+ 13Vand–13VforR$_L$>2KΩ
16. Outputshort-circuitcurrent:25mA
17. Supply current:28mA
18. Power consumption:85MW
19. Transient response: risetime=0.3μs
    Overshoot=5%

APPENDIX–C

Pin Configuration:

IC555



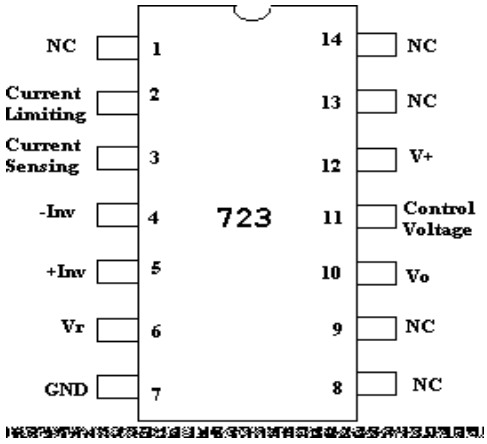
Specifications:

1. Operating temperature: SE555-55°Cto125°C
   NE5550°to70°C
2. Supply voltage : +5V to+18V
3. Timing : µ SectoHours
4. Sink current : 200mA
5. Temperature stability : 50PPM/°C change in temp or 0-005%/°C.

APPENDIX–D

IC723

Pin Configuration:



Specificationsof723:

Power dissipation	:	1W
Input Voltage	:	9.5 to
40V Output Voltage:		2to37V
Output Current	:	150mA for Vin-Vo=3V
		10mA for Vin-Vo=
38V Load regulation		:0.6% Vo
Line regulation	:	0.5%Vo

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