CSE/IT 212 (R-15)

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II/IV B.Tech. DEGREE EXAMINATIONS, NOVEMBER- 2019

First Semester

CSE/IT

DIGITAL LOGIC DESIGN

Time: Three Hours **Maximum marks:60**

Answer Question No.1 Compulsory **6X2=12 M**

Answer ONE Question from each Unit **4X12=48 M**

1. a) Explain Demorgans' Laws with suitable truth tables
   b) Convert the decimal number 250.5 to binary, and octal
   c) Brief on MSI
   d) Purpose of excitation tables.
   e) Define counter
   f) Mention types of ROMs

UNIT-I

2. a) Convert $(615.25)_8$ to its hexadecimal equivalent
   b) Convert $(12.125)_{10}$ into binary.
   c) Reduce the following Boolean Expressions.
   i) $AB + A(B+C) + B'(B+D)$ ii) $A+B+A'B'C$

(OR)

3. a) Perform the following subtraction:
   $(11010)_2 - (10000)_2$ using 1's complement
   $(1000100)_2 - (1010100)_2$ using 2's complement
   b) Obtain the Dual of the following Boolean expressions
   i) $x'yz' + x'yz' + xy'z' + xy'z$ ii) $x'yz + xy'z' + xyz + xyz'$
   c) Obtain the simplified expression in SOP form for the following using K-map method. F(A,B,C,D)= (0,1,4,5,16,17,21,25,29)

P.T.O

UNIT-II

4. Give the design of a full adder and explain the design of four bit parallel adder.

(OR)

5. Explain the process of multiplying two binary numbers having J and K bits each. Give the design and explain the circuit to perform binary multiplication using two binary numbers having 3 and 4 bits each.

UNIT-III

6. Define flip-flop and explain the functioning of a edge triggered JK flip flop. Give the characteristic table for the same.

(OR)

7. Explain the design of D Flip Flop with Present and Clear. Give a brief on edge triggering Vs Level Clocking and give an example timing diagram for the functioning of the D Flip Flop with Present and Clear.

UNIT-IV

8. Define register. Which flip flop is most suitable for the design of register and why? Design a 4 bit shift register which performs left and right shift based on the option chosen.

(OR)

9. a) Explain the design of 4 bit ripple counter.
   b) Give a brief on PLA and PAL.

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II/IV B.Tech. (Supple) DEGREE EXAMINATIONS, JUNE- 2019

First Semester

CSE/IT

DIGITAL LOGIC DESIGN

Time: Three Hours **Maximum marks:60**

Answer Question No.1 Compulsory **6X2=12 M**

Answer ONE Question from each Unit **4X12=48 M**

1. a) Prime Implicants
   b) Hold time and Propagation delay time
   c) Purpose of state table state digram
   d) MSI and LSI
   e) Design of T FlipFlop
   f) Brief on characteristic features of EPROM and EEPROM

UNIT-I

2. a) Obtain the complement of the following Boolean expressions.
   i) A'C'+ABC+AC' ii) (x'y'+z)'+z+xy+wz
   iii) A'B(D'+C'D)+B(A+A'CD) iv) (A'+C)(A'+C')(A+B+C'D)
   b) Draw the multiple level NOR circuit for the following expression: A(B+C+D)+BCD

(OR)

3. a) Obtain minimal SOP expression for the given Boolean function, using K-map: F(A,B,C,D)= $\sum$(0,1,4,6,8,9,10,12)+D(3,7,13,14,15). And draw the circuit using 2-input NAND gates.
   b) Express the following function in sum of minterms and product of maxterms: F(A,B,C,D)=B D+A D+BD.

UNIT-II

4. a) Implement a Boolean function F(x,y,z)= $\sum$(2,4,6) with a Multiplexer.

P.T.O

b) Design a full-subtractor circuit with three inputs x,y,z and outputs D,B. The circuit subtracts X-Y-Z where Z is the input borrow, B is the output borrow and D is the difference draw the circuit using NAND gates.

(OR)

5. a) Implement 64x1 multiplexer with four 16x1 and one 4x1 multiplexer. (Use only block diagram)

b) A combinational logic circuit is defined by the following Boolean functions. F1=(ABC)'+AC F2=A(BC)'+A'B F3=AB'C+AB
Design the circuit with a decoder and external gates.

UNIT-III

6. Define FlipFlop and explain the concept of edge triggered FlipFlop. Convert the following:

i) J-K flip-flop to T-flip-flop ii) R-S flip-flop to J-K- flip-flo
iii) J-K flip-flop to D-flip-flop

(OR)

7. a) Draw tha circuit diagram of clocked D-flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.

b) Explain the procedure for the design of sequential circuits with example.

UNIT-IV

8. Derive the PLA programming table and the PLA structure for the combinational circuit that squares a 3-bit number. Minimize the number of product terms.

(OR)

9. a) Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram.

b) Draw and explain functioning of 4-bit universal shift register with suitable diagram.